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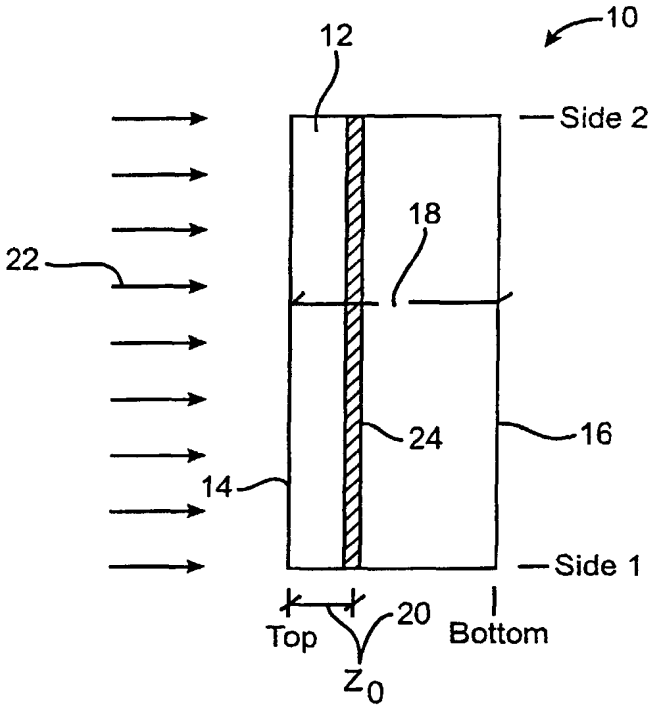
(54) Title: TREATMENT METHOD OF CLEAVED FILM FOR THE MANUFACTURE OF SUBSTRATES

(57) Abstract

A method for treating a film of material, which can be defined on a substrate (10), e.g., silicon. The method includes providing a substrate (10) comprising a cleaved surface (12), which is characterized by a predetermined surface roughness value. The substrate (10) also has a distribution of hydrogen bearing particles (22) defined from the cleaved surface (12) to a region underlying said cleaved surface (24). The method also includes increasing a temperature of the cleaved surface (12) to greater than about 1000 Degrees Celsius while maintaining the cleaved surface (12) in a etchant bearing environment to reduce the predetermined surface roughness value by about fifty percent and greater. Preferably, the value can be reduced by about eighty or ninety percent and greater, depending upon the embodiment.



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TREATMENT METHOD OF CLEAVED FILM FOR THE MANUFACTURE OF SUBSTRATES

BACKGROUND OF THE INVENTION

The present invention relates to the manufacture of objects. More particularly, the present invention provides a technique for improving surface texture or surface characteristics of a film of material, e.g., silicon, silicon germanium, or others. The present invention can be applied to treating or smoothing a cleaved film from a layer transfer process for the manufacture of integrated circuits, for example. But it will be recognized that the invention has a wider range of applicability; it can also be applied to smoothing a film for other substrates such as multi-layered integrated circuit devices, three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, microelectromechanical systems ("MEMS"), sensors, actuators, solar cells, flat panel displays (e.g., LCD, AMLCD), doping semiconductor devices, biological and biomedical devices, and the like.

Integrated circuits are fabricated on chips of semiconductor material. These integrated circuits often contain thousands, or even millions, of transistors and other devices. In particular, it is desirable to put as many transistors as possible within a given area of semiconductor because more transistors typically provide greater functionality, and a smaller chip means more chips per wafer and lower costs. Some integrated circuits are fabricated on a slice or wafer, of single-crystal (monocrystalline) silicon, commonly termed a "bulk" silicon wafer. Devices on such "bulk" silicon wafer typically are isolated from each other. A variety of techniques have been proposed or used to isolate these devices from each other on the bulk silicon wafer, such as a local oxidation of silicon ("LOCOS") process, trench isolation, and others. These techniques, however, are not free from limitations. For example, conventional isolation techniques consume a considerable amount of valuable wafer surface area on the chip, and often generate a non-planar surface as an artifact of the isolation process. Either or both of these considerations generally limit the degree of integration achievable in a given chip. Additionally, trench isolation often requires a process of reactive ion etching, which is extremely time consuming and can be difficult to achieve accurately.

An approach to achieving very-large scale integration ("VLSI") or ultra-large scale integration ("ULSI") is by using a semiconductor-on-insulator ("SOI") wafer. An SOI wafer typically has a layer of silicon on top of a layer of an insulator material. A variety of techniques have been proposed or used for fabricating the SOI wafer. These techniques include, among others, growing a thin layer of silicon on a sapphire substrate, bonding a layer of silicon to an insulating substrate, and forming an insulating layer beneath a silicon layer in a bulk silicon wafer. In an SOI integrated circuit, essentially complete device isolation is often achieved using conventional device processing methods by surrounding each device, including the bottom of the device, with an insulator. An advantage SOI wafers have over bulk silicon wafers is that the area required for isolation between devices on an SOI wafer is less than the area typically required for isolation on a bulk silicon wafer.

SOI offers other advantages over bulk silicon technologies as well. For example, SOI offers a simpler fabrication sequence compared to a bulk silicon wafer. Devices fabricated on an SOI wafer may also have better radiation resistance, less photo-induced current, and less cross-talk than devices fabricated on bulk silicon wafers. Many problems, however, that have already been solved regarding fabricating devices on bulk silicon wafers remain to be solved for fabricating devices on SOI wafers.

For example, SOI wafers generally must also be polished to remove any surface irregularities from the film of silicon overlying the insulating layer. Polishing generally includes, among others, chemical mechanical polishing, commonly termed CMP. CMP is generally time consuming and expensive, and can be difficult to perform cost efficiently to remove surface non-uniformities. That is, a CMP machine is expensive and requires large quantities of slurry mixture, which is also expensive. The slurry mixture can also be highly acidic or caustic. Accordingly, the slurry mixture can influence functionality and reliability of devices that are fabricated on the SOI wafer.

From the above, it is seen that an improved technique for manufacturing a substrate such as an SOI wafer is highly desirable.

SUMMARY OF THE INVENTION

According to the present invention, a technique for treating a film of material is provided. More particularly, the present invention provides a method for treating a cleaved surface and/or an implanted surface using a combination of thermal

treatment and chemical reaction, which can form a substantially smooth film layer from the cleaved surface.

In a specific embodiment, the present invention provides a method for fabricating a substrate, e.g., silicon, silicon-on-insulator, silicon-on-silicon, and many others. The method includes providing a donor substrate comprising an upper surface. The method also includes introducing a plurality of particles (e.g., hydrogen, mixtures of hydrogen, helium/hydrogen, halogen/hydrogen) through the upper surface and into the donor substrate to a selected depth beneath the upper surface to define a thickness of material of the donor substrate defined from the upper surface to the selected depth. The plurality of particles are defined by a distribution along the selected depth, which ranges from a greater or maximum value to a reduced value. Next, energy is introduced to the donor substrate to initiate a cleaving action to free the thickness of material from the donor substrate to define a cleaved surface from the donor substrate. The cleaved surface has a surface roughness of a predetermined value, which is generally undesirable. The surface also has a portion of the distribution of the plurality of particles defined therein. The method also includes applying thermal treatment and an etchant (or deposition material or combination of etchant and deposition material) to the cleaved surface and the portion of the distribution of the plurality of particles to reduce the surface roughness from the predetermined value.

In an alternative embodiment, the present invention provides a semiconductor substrate. The substrate includes a cleaved surface, which is characterized by a predetermined surface roughness value. A distribution of hydrogen bearing particles are defined from the cleaved surface to a region underlying the cleaved film. The distribution of hydrogen particles assist in surface treatment of the cleaved film during subsequent heat treatment processes or the like. The substrate can be a semiconductor substrate as well as other types of substrates.

In a specific embodiment, the present invention provides a method for forming a semiconductor substrate. The method includes forming a first porous silicon layer on at least one surface of a silicon substrate; and forming a second layer having a larger porosity than the first porous silicon layer at a constant depth from a surface of the porous silicon in the first porous silicon layer. The second layer forming step comprising implanting ions into the first porous silicon layer with a given projection range. The method also includes bonding the non-porous layer and a support substrate together.

Next, the method includes a step of separating the silicon substrate into two portions at the second layer to remove the porous silicon layer exposed on a surface of the support substrate and exposing the non-porous layer. The method includes smoothing the non-porous layer by subjecting surface(s) of the non-porous layer using an etchant species (e.g., HCl) and thermal treatment. The present substrate can be maintained at 1 atmosphere in some embodiments.

In a specific embodiment, the present invention provides a novel process for smoothing a surface of a separated film. The present process is for the preparation of thin semiconductor material films. The process includes a step of implanting by ion bombardment of the face of the wafer by means of ions creating in the volume of the wafer at a depth close to the average penetration depth of the ions, where a layer of gaseous microbubbles defines the volume of the wafer a lower region constituting a majority of the substrate and an upper region constituting the thin film. A temperature of the wafer during implantation is kept below the temperature at which the gas produced by the implanted ions can escape from the semiconductor by diffusion. The process also includes contacting the planar face of the wafer with a stiffener constituted by at least one rigid material layer. The process includes treating the assembly of the wafer and the stiffener at a temperature above that at which the ion bombardment takes place and adequate to create by a crystalline rearrangement effect in the wafer and a pressure effect in the microbubbles to create separation between the thin film and the majority of the substrate. The stiffener and the planar face of the wafer are kept in intimate contact during the stage to free the thin film from the majority of the substrate. The method also includes applying a combination of thermal treatment and an etchant to the thin film to reduce a surface roughness of the thin film to a predetermined value.

Numerous benefits are achieved by way of the present invention over pre-existing techniques. For example, the present invention provides an efficient technique for forming a substantially uniform surface on an SOI wafer. Additionally, the substantially uniform surface is made by way of common hydrogen treatment and etching techniques, which can be found in conventional epitaxial tools. Furthermore, the present invention provides a novel uniform layer, which can be ready for the manufacture of integrated circuits. The present invention also relies upon standard fabrication gases such as HCl and hydrogen gas. In preferred embodiments, the present

invention can improve bond interface integrity, improve crystal structure, and reduce defects in the substrate simultaneously during the process. Depending upon the embodiment, one or more of these benefits is present. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

These and other embodiments of the present invention, as well as its advantages and features are described in more detail in conjunction with the text below and attached Figs.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1-11 are simplified diagrams illustrating a controlled cleaving technique according to an embodiment of the present invention; and

Figs. 12-16 are simplified cross-sectional view diagrams illustrating a method of forming a silicon-on-insulator substrate according to the present invention.

Figs. 17A to 17D are schematic diagrams for explaining a semiconductor substrate producing process according to an embodiment of the present invention;

Figs. 18A to 18G are schematic diagrams for explaining a semiconductor substrate producing process according to an embodiment of the present invention;

Figs. 19A to 19F are schematic diagrams for explaining a semiconductor substrate producing process according to an embodiment of the present invention;

Figs. 20A to 20E are schematic diagrams for explaining a semiconductor substrate producing process according to an embodiment of the present invention;

Figs. 21A to 21G are schematic diagrams for explaining a semiconductor substrate producing process according to an embodiment of the present invention;

Figs. 22A and 22B are schematic diagrams for explaining a semiconductor substrate producing process according to an embodiment of the present invention; and

Figs. 23A and 23B are simplified side-view diagrams of anodization systems according to an embodiment of the present invention

Fig. 24 is a simplified diagram of a concentration profile of the hydrogen ions as a function of the penetration depth according to an embodiment of the present invention;

Fig. 25 is a simplified diagram of a monocrystalline semiconductor wafer used in the invention as the origin of the monocrystalline film, in section, exposed to a bombardment of H + ions and within which has appeared a gas microbubble layer produced by the implanted particles;

Fig. 26 is a simplified diagram of a semiconductor wafer shown in Fig. 25 and covered with a stiffener;

Fig. 27 is a simplified diagram of an assembly of the semiconductor wafer and the stiffener shown in Fig. 26 at the end of the heat treatment phase, when cleaving has taken place between the film and the substrate mass;

Fig. 28 is a simplified diagram of a removed film attached to a stiffener according to an embodiment of the present invention; and

Fig. 29 is a simplified diagram of a smoothed film attached to a stiffener according to an embodiment of the present invention

DESCRIPTION OF THE SPECIFIC EMBODIMENT

According to the present invention, a technique for treating a film of material is provided. More particularly, the present invention provides a method for treating a cleaved surface and/or an implanted surface using a combination of thermal treatment and chemical reaction, which can form a substantially smooth film layer from the cleaved surface. The invention will be better understood by reference to the Figs. and the descriptions below.

Fig. 1 is a simplified cross-sectional view diagram of a substrate 10 according to the present invention. The diagram is merely an illustration and should not limit the scope of the claims herein. As merely an example, substrate 10 is a silicon wafer which includes a material region 12 to be removed, which is a thin relatively uniform film derived from the substrate material. The silicon wafer 10 includes a top surface 14, a bottom surface 16, and a thickness 18. Substrate 10 also has a first side (side 1) and a second side (side 2) (which are also referenced below in the Figs.). Material region 12 also includes a thickness 20, within the thickness 18 of the silicon

wafer. The present invention provides a novel technique for removing the material region 12 using the following sequence of steps.

Selected energetic particles implant 22 through the top surface 14 of the silicon wafer to a selected depth 24, which defines the thickness 20 of the material region 12, termed the thin film of material. A variety of techniques can be used to implant the energetic particles into the silicon wafer. These techniques include ion implantation using, for example, beam line ion implantation equipment manufactured from companies such as Applied Materials, Eaton Corporation, Varian, and others. Alternatively, implantation occurs using a plasma immersion ion implantation ("PIII") technique. Examples of plasma immersion implantation techniques are described in "Recent Applications of Plasma Immersion Ion Implantation," Paul K. Chu, Chung Chan, and Nathan W. Cheung, SEMICONDUCTOR INTERNATIONAL, pp. 165-172, June 1996, and "Plasma Immersion Ion Implantation - A Fledgling Technique for Semiconductor Processing,", P.K. Chu, S. Qin, C. Chan, N.W. Cheung, and L.A. Larson, MATERIAL SCIENCE AND ENGINEERING REPORTS, A Review Journal, pp. 207-280, Volume R17, Nos. 6-7, (Nov. 30, 1996), which are both hereby incorporated by reference for all purposes. Furthermore, implantation can occur using ion shower. Of course, techniques used depend upon the application.

Depending upon the application, smaller mass particles are generally selected to reduce a possibility of damage to the material region 12. That is, smaller mass particles easily travel through the substrate material to the selected depth without substantially damaging the material region that the particles traverse through. For example, the smaller mass particles (or energetic particles) can be almost any charged (e.g., positive or negative) and/or neutral atoms or molecules, or electrons, or the like. In a specific embodiment, the particles can be neutral and/or charged particles including ions such as ions of hydrogen and its isotopes, rare gas ions such as helium and its isotopes, and neon. The particles can also be derived from compounds such as gases, e.g., hydrogen gas, water vapor, methane, and hydrogen compounds, and other light atomic mass particles. Alternatively, the particles can be any combination of the above particles, and/or ions and/or molecular species and/or atomic species. The particles

generally have sufficient kinetic energy to penetrate through the surface to the selected depth underneath the surface.

In other embodiments, the particles can be introduced by way of injection. That is, the particles can be introduced to a selected region of the substrate by diffusion. Alternatively, the particles can be introduced by a combination of implantation and diffusion. Still further, the particles can be larger sized, such as silicon or the like. The particles can be smaller and larger sized, depending upon the application. The particles can be almost any suitable species that can be effectively introduced into the selected region for cleaving purposes.

Using hydrogen as the implanted species into the silicon wafer as an example, the implantation process is performed using a specific set of conditions. Implantation dose ranges from about 10^{15} to about 10^{18} atoms/cm^2, and preferably the dose is greater than about 10^{16} atoms/cm^2. Implantation energy ranges from about 1 KeV to about 1 MeV , and is generally about 50 KeV. Implantation temperature ranges from about -200 to about 600 Degrees Celsius, and is preferably less than about 400 Degrees Celsius to prevent a possibility of a substantial quantity of hydrogen ions from diffusing out of the implanted silicon wafer and annealing the implanted damage and stress. The hydrogen ions can be selectively introduced into the silicon wafer to the selected depth at an accuracy of about +/- 0.03 to +/- 0.05 microns. Of course, the type of ion used and process conditions depend upon the application.

Effectively, the implanted particles add stress or reduce fracture energy along a plane parallel to the top surface of the substrate at the selected depth. The energies depend, in part, upon the implantation species and conditions. These particles reduce a fracture energy level of the substrate at the selected depth. This allows for a controlled cleave along the implanted plane at the selected depth. Implantation can occur under conditions such that the energy state of substrate at all internal locations is insufficient to initiate a non-reversible fracture (i.e., separation or cleaving) in the substrate material. It should be noted, however, that implantation may cause a certain amount of defects (e.g., micro-detects) in the substrate that can be repaired by subsequent heat treatment, e.g., thermal annealing or rapid thermal annealing.

Fig. 1A is a simplified particle distribution diagram 250 according to an embodiment of the present invention. The diagram is merely an example that should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The diagram 250 shows concentration of particles, which is on the vertical axis, against spatial distribution along a depth of the substrate, which is on the horizontal axis. As shown, the spatial distribution ranges from the top 253 of the substrate to the selected depth (z_o) to the bottom of the substrate 257. The concentration distribution is shown by the line 251, which has a maximum value 253. The maximum value is defined as C_{MAX} 259. The maximum value is defined at the selected depth. Depending upon the embodiment, other implant profiles can also be provided.

Fig. 2 is a simplified energy diagram 200 along a cross-section of the implanted substrate 10 according to the present invention. The diagram is merely an illustration and should not limit the scope of the claims herein. The simplified diagram includes a vertical axis 201 that represents an energy level (E) (or additional energy) to cause a cleave in the substrate. A horizontal axis 203 represents a depth or distance from the bottom of the wafer to the top of the wafer. After implanting particles into the wafer, the substrate has an average cleave energy represented as E 205, which is the amount of energy needed to cleave the wafer along various cross-sectional regions along the wafer depth. The cleave energy (E_c) is equal to the bulk material fracture energy (E_{mat}) in non-implanted regions. At the selected depth 20, energy (E_{cz}) 207 is lower since the implanted particles essentially break or weaken bonds in the crystalline structure (or increase stress caused by a presence of particles also contributing to lower energy (E_{cz}) 207 of the substrate) to lower the amount of energy needed to cleave the substrate at the selected depth. The present invention takes advantage of the lower energy (or increased stress) at the selected depth to cleave the thin film in a controlled manner.

Substrates, however, are not generally free from defects or "weak" regions across the possible cleave front or selected depth zo after the implantation process. In these cases, the cleave generally cannot be controlled, since they are subject to random variations such as bulk material non-uniformities, built-in stresses, defects,

and the like. Fig. 3 is a simplified energy diagram 300 across a cleave front for the implanted substrate 10 having these defects. The diagram 300 is merely an illustration and should not limit the scope of the claims herein. The diagram has a vertical axis 301 which represents additional energy (E) and a horizontal axis 303 which represents a distance from side 1 to side 2 of the substrate, that is, the horizontal axis represents regions along the cleave front of the substrate. As shown, the cleave front has two regions 305 and 307 represented as region 1 and region 2, respectively, which have cleave energies less than the average cleave energy (E_{cz}) 207 (possibly due to a higher concentration of defects or the like). Accordingly, it is highly likely that the cleave process begins at one or both of the above regions, since each region has a lower cleave energy than surrounding regions.

An example of a cleave process for the substrate illustrated by the above Fig. is described as follows with reference to Fig. 4. Fig. 4 is a simplified top-view diagram 400 of multiple cleave fronts 401, 403 propagating through the implanted substrate. The cleave fronts originate at "weaker" regions in the cleave plane, which specifically includes regions 1 and 2. The cleave fronts originate and propagate randomly as shown by the arrows. A limitation with the use of random propagation among multiple cleave fronts is the possibility of having different cleave fronts join along slightly different planes or the possibility of forming cracks, which is described in more detail below.

Fig. 5 is a simplified cross-sectional view 500 of a film cleaved from a wafer having multiple cleave fronts at, for example, regions 1 305 and 2 307. This diagram is merely an illustration and should not limit the scope of the claims herein. As shown, the cleave from region 1 joined with the cleave from region 2 at region 3 309, which is defined along slightly different planes, may initiate a secondary cleave or crack 311 along the film. Depending upon the magnitude of the difference 313, the film may not be of sufficient quality for use in manufacture of substrates for integrated circuits or other applications. A substrate having crack 311 generally cannot be used for processing. Accordingly, it is generally undesirable to cleave a wafer using multiple fronts in a random manner. An example of a technique which may form multiple cleave fronts in a random manner is described in U.S. Patent No. 5,374,564, which is

in the name of Michel Bruel ("Bruel"), and assigned to Commissariat A l'Energie Atomique in France. Bruel generally describes a technique for cleaving an implanted wafer by global thermal treatment (i.e., thermally treating the entire plane of the implant) using thermally activated diffusion. Global thermal treatment of the substrate generally causes an initiation of multiple cleave fronts which propagate independently. In general, Bruel discloses a technique for an "uncontrollable" cleaving action by way of initiating and maintaining a cleaving action by a global thermal source, which may produce undesirable results. These undesirable results include potential problems such as an imperfect joining of cleave fronts, an excessively rough surface finish on the surface of the cleaved material since the energy level for maintaining the cleave exceeds the amount required, and many others. The present invention overcomes the formation of random cleave fronts by a controlled distribution or selective positioning of energy on the implanted substrate.

Fig. 6 is a simplified cross-sectional view of an implanted substrate 10 using selective positioning of cleave energy according to the present invention. This diagram is merely an illustration, and should not limit the scope of the claims herein. The implanted wafer undergoes a step of selective energy placement 601 or positioning or targeting which provides a controlled cleaving action of the material region 12 at the selected depth 603. In preferred embodiments, selected energy placement 607 occurs near an edge or corner region of the selected depth 603 of substrate 10. The impulse (or impulses) is provided using energy sources. Examples of sources include, among others, a chemical source, a mechanical source, an electrical source, and a thermal sink or source. The chemical source can include a variety such as particles, fluids, gases, or liquids. These chemical sources can also include chemical reaction to increase stress in the material region. The chemical source is introduced as flood, time-varying, spatially varying, or continuous. In other embodiments, a mechanical source is derived from rotational, translational, compressional, expansional, or ultrasonic energies. The mechanical source can be introduced as flood, time-varying, spatially varying, or continuous. In further embodiments, the electrical source is selected from an applied voltage or an applied electro-magnetic field, which is introduced as flood, time-varying, spatially varying, or continuous. In still further embodiments, the thermal source or

sink is selected from radiation, convection, or conduction. This thermal source can be selected from, among others, a photon beam, a fluid jet, a liquid jet, a gas jet, an electro/magnetic field, an electron beam, a thermo-electric heating, a furnace, and the like. The thermal sink can be selected from a fluid jet, a liquid jet, a gas jet, a cryogenic fluid, a super-cooled liquid, a thermo-electric cooling means, an electro/magnetic field, and others. Similar to the previous embodiments, the thermal source is applied as flood, time-varying, spatially varying, or continuous. Still further, any of the above embodiments can be combined or even separated, depending upon the application. Of course, the type of source used depends upon the application.

In a specific embodiment, the energy source can be a fluid jet that is pressurized (e.g., compressional) according to an embodiment of the present invention. Fig. 6A shows a simplified cross-sectional view diagram of a fluid jet from a fluid nozzle 608 used to perform the controlled cleaving process according to an embodiment of the present invention. The fluid jet 607 (or liquid jet or gas jet) impinges on an edge region of substrate 10 to initiate the controlled cleaving process. The fluid jet from a compressed or pressurized fluid source is directed to a region at the selected depth 603 to cleave a thickness of material region 12 from substrate 10 using force, e.g., mechanical, chemical, thermal. As shown, the fluid jet separates substrate 10 into two regions, including region 609 and region 611 that separate from each other at selected depth 603. The fluid jet can also be adjusted to initiate and maintain the controlled cleaving process to separate material 12 from substrate 10. Depending upon the application, the fluid jet can be adjusted in direction, location, and magnitude to achieve the desired controlled cleaving process. The fluid jet can be a liquid jet or a gas jet or a combination of liquid and gas.

In a preferred embodiment, the energy source can be a compressional source such as, for example, compressed fluid that is static. Fig. 6B shows a simplified cross-sectional view diagram of a compressed fluid source 607 according to an embodiment of the present invention. The compressed fluid source 607 (e.g., pressurized liquid, pressurized gas) is applied to a sealed chamber 621, which surrounds a periphery or edge of the substrate 10. As shown, the chamber is enclosed by device 623, which is sealed by, for example, o-rings 625 or the like, and which surrounds the

outer edge of the substrate. The chamber has a pressure maintained at PC that is applied to the edge region of substrate 10 to initiate the controlled cleaving process at the selected depth of implanted material. The outer surface or face of the substrate is maintained at pressure PA which can be ambient pressure, e.g., 1 atmosphere or less. A pressure differential exists between the pressure in the chamber, which is higher, and the ambient pressure. The pressure difference applies force to the implanted region at the selected depth 603. The implanted region at the selected depth is structurally weaker than surrounding regions, including any bonded regions. Force is applied via the pressure differential until the controlled cleaving process is initiated. The controlled cleaving process separates the thickness of material 609 from substrate material 611 to split the thickness of material from the substrate material at the selected depth. Additionally, pressure PC forces material region 12 to separate by a "prying action" from substrate material 611. During the cleaving process, the pressure in the chamber can also be adjusted to initiate and maintain the controlled cleaving process to separate material 12 from substrate 10. Depending upon the application, the pressure can be adjusted in magnitude to achieve the desired controlled cleaving process. The fluid pressure can be derived from a liquid or a gas or a combination of liquid and gas.

In a specific embodiment, the present invention provides a resulting substrate 611, 12 that has a cleaved surface 627. The cleaved surface has a certain or predetermined amount of surface roughness. The surface roughness is often greater than that which is generally acceptable for manufacturing integrated circuits. In silicon wafers, for example, the surface roughness is generally about 10 nanometers root mean square ("RMS") or greater. Alternatively, the surface roughness is about 2-8 nanometers root mean square and greater. Each of the cleaved surfaces has a particle concentration, which is shown in the diagram in reference numeral 629. The concentration of particles at a maximum is generally at the selected depth (z_o). The particle concentration can be hydrogen, for example, or other hydrogen bearing compounds. The hydrogen bearing compound will assist in annealing the cleaved surface in later processing steps.

In a specific embodiment, the present invention provides a controlled-propagating cleave. The controlled-propagating cleave uses multiple successive

impulses to initiate and perhaps propagate a cleaving process 700, as illustrated by Fig. 7. This diagram is merely an illustration, and should not limit the scope of the claims herein. As shown, the impulse is directed at an edge of the substrate, which propagates a cleave front toward the center of the substrate to remove the material layer from the substrate. In this embodiment, a source applies multiple pulses (i.e., pulse 1, 2, and 3) successively to the substrate. Pulse 1 701 is directed to an edge 703 of the substrate to initiate the cleave action. Pulse 2 705 is also directed at the edge 707 on one side of pulse 1 to expand the cleave front. Pulse 3 709 is directed to an opposite edge 711 of pulse 1 along the expanding cleave front to further remove the material layer from the substrate. The combination of these impulses or pulses provides a controlled cleaving action 713 of the material layer from the substrate.

Fig. 8 is a simplified illustration of selected energies 800 from the pulses in the preceding embodiment for the controlled-propagating cleave. This diagram is merely an illustration, and should not limit the scope of the claims herein. As shown, the pulse 1 has an energy level which exceeds average cleaving energy (E), which is the necessary energy for initiating the cleaving action. Pulses 2 and 3 are made using lower energy levels along the cleave front to maintain or sustain the cleaving action. In a specific embodiment, the pulse is a laser pulse where an impinging beam heats a selected region of the substrate through a pulse and a thermal pulse gradient causes supplemental stresses which together exceed cleave formation or propagation energies, which create a single cleave front. In preferred embodiments, the impinging beam heats and causes a thermal pulse gradient simultaneously, which exceed cleave energy formation or propagation energies. More preferably, the impinging beam cools and causes a thermal pulse gradient simultaneously, which exceed cleave energy formation or propagation energies.

Optionally, a built-in energy state of the substrate or stress can be globally raised toward the energy level necessary to initiate the cleaving action, but not enough to initiate the cleaving action before directing the multiple successive impulses to the substrate according to the present invention. The global energy state of the substrate can be raised or lowered using a variety of sources such as chemical, mechanical, thermal (sink or source), or electrical, alone or in combination. The

chemical source can include a variety such as particles, fluids, gases, or liquids. These sources can also include chemical reaction to increase stress in the material region. The chemical source is introduced as flood, time-varying, spatially varying, or continuous.

In other embodiments, a mechanical source is derived from rotational, translational, compressional, expansional, or ultrasonic energies. The mechanical source can be introduced as flood, time-varying, spatially varying, or continuous. In further embodiments, the electrical source is selected from an applied voltage or an applied electro-magnetic field, which is introduced as flood, time-varying, spatially varying, or continuous. In still further embodiments, the thermal source or sink is selected from radiation, convection, or conduction. This thermal source can be selected from, among others, a photon beam, a fluid jet, a liquid jet, a gas jet, an electro/magnetic field, an electron beam, a thermo-electric heating, and a furnace. The thermal sink can be selected from a fluid jet, a liquid jet, a gas jet, a cryogenic fluid, a super-cooled liquid, a thermo-electric cooling means, an electro/magnetic field, and others. Similar to the previous embodiments, the thermal source is applied as flood, time-varying, spatially varying, or continuous. Still further, any of the above embodiments can be combined or even separated, depending upon the application. Of course, the type of source used also depends upon the application. As noted, the global source increases a level of energy or stress in the material region without initiating a cleaving action in the material region before providing energy to initiate the controlled cleaving action.

In a specific embodiment, an energy source elevates an energy level of the substrate cleave plane above its cleave front propagation energy but is insufficient to cause self-initiation of a cleave front. In particular, a thermal energy source or sink in the form of heat or lack of heat (e.g., cooling source) can be applied globally to the substrate to increase the energy state or stress level of the substrate without initiating a cleave front. Alternatively, the energy source can be electrical, chemical, or mechanical. A directed energy source provides an application of energy to a selected region of the substrate material to initiate a cleave front which self-propagates through the implanted region of the substrate until the thin film of material is removed. A

variety of techniques can be used to initiate the cleave action. These techniques are described by way of the Figs. below.

Fig. 9 is a simplified illustration of an energy state 900 for a controlled cleaving action using a single controlled source according to an aspect of the present invention. This diagram is merely an illustration, and should not limit the scope of the claims herein. In this embodiment, the energy level or state of the substrate is raised using a global energy source above the cleave front propagation energy state, but is lower than the energy state necessary to initiate the cleave front. To initiate the cleave front, an energy source such as a laser directs a beam in the form of a pulse at an edge of the substrate to initiate the cleaving action. Alternatively, the energy source can be a cooling fluid (e.g., liquid, gas) that directs a cooling medium in the form of a pulse at an edge of the substrate to initiate the cleaving action. The global energy source maintains the cleaving action which generally requires a lower energy level than the initiation energy.

An alternative aspect of the invention is illustrated by Figs. 10 and 11. Fig. 10 is a simplified illustration of an implanted substrate 1000 undergoing rotational forces 1001, 1003. This diagram is merely an illustration, and should not limit the scope of the claims herein. As shown, the substrate includes a top surface 1005, a bottom surface 1007, and an implanted region 1009 at a selected depth. An energy source increases a global energy level of the substrate using a light beam or heat source to a level above the cleave front propagation energy state, but lower than the energy state necessary to initiate the cleave front. The substrate undergoes a rotational force turning clockwise 1001 on top surface and a rotational force turning counter-clockwise 1003 on the bottom surface which creates stress at the implanted region 1009 to initiate a cleave front. Alternatively, the top surface undergoes a counter-clockwise rotational force and the bottom surface undergoes a clockwise rotational force. Of course, the direction of the force generally does not matter in this embodiment.

Fig. 11 is a simplified diagram of an energy state 1100 for the controlled cleaving action using the rotational force according to the present invention. This diagram is merely an illustration, and should not limit the scope of the claims herein. As previously noted, the energy level or state of the substrate is raised using a global

energy source (e.g., thermal, beam) above the cleave front propagation energy state, but is lower than the energy state necessary to initiate the cleave front. To initiate the cleave front, a mechanical energy means such as rotational force applied to the implanted region initiates the cleave front. In particular, rotational force applied to the implanted region of the substrates creates zero stress at the center of the substrate and greatest at the periphery, essentially being proportional to the radius. In this example, the central initiating pulse causes a radially expanding cleave front to cleave the substrate.

The removed material region provides a thin film of silicon material for processing. The silicon material possesses limited surface roughness and desired planarity characteristics for use in a silicon-on-insulator substrate. In certain embodiments, the surface roughness of the detached film has features that are less than about 60 nm, or less than about 40 nm, or less than about 20 nm. Accordingly, the present invention provides thin silicon films which can be smoother and more uniform than pre-existing techniques.

In a preferred embodiment, the present invention is practiced at temperatures that are lower than those used by pre-existing techniques. In particular, the present invention does not require increasing the entire substrate temperature to initiate and sustain the cleaving action as pre-existing techniques. In some embodiments for silicon wafers and hydrogen implants, substrate temperature does not exceed about 400 Degrees Celsius during the cleaving process. Alternatively, substrate temperature does not exceed about 350 Degrees Celsius during the cleaving process. Alternatively, substrate temperature is kept substantially below implanting temperatures via a thermal sink, e.g., cooling fluid, cryogenic fluid. Accordingly, the present invention reduces a possibility of unnecessary damage from an excessive release of energy from random cleave fronts, which generally improves surface quality of a detached film(s) and/or the substrate(s). Accordingly, the present invention provides resulting films on substrates at higher overall yields and quality.

The above embodiments are described in terms of cleaving a thin film of material from a substrate. The substrate, however, can be disposed on a workpiece such as a stiffener or the like before the controlled cleaving process. The workpiece

joins to a top surface or implanted surface of the substrate to provide structural support to the thin film of material during controlled cleaving processes. The workpiece can be joined to the substrate using a variety of bonding or joining techniques, e.g., electro-statics, adhesives, interatomic. Some of these bonding techniques are described herein. The workpiece can be made of a dielectric material (e.g., quartz, glass, sapphire, silicon nitride, silicon dioxide), a conductive material (silicon, silicon carbide, polysilicon, group III/V materials, metal), and plastics (e.g., polyimide-based materials). Of course, the type of workpiece used will depend upon the application.

Alternatively, the substrate having the film to be detached can be temporarily disposed on a transfer substrate such as a stiffener or the like before the controlled cleaving process. The transfer substrate joins to a top surface or implanted surface of the substrate having the film to provide structural support to the thin film of material during controlled cleaving processes. The transfer substrate can be temporarily joined to the substrate having the film using a variety of bonding or joining techniques, e.g., electro-statics, adhesives, interatomic. Some of these bonding techniques are described herein. The transfer substrate can be made of a dielectric material (e.g., quartz, glass, sapphire, silicon nitride, silicon dioxide), a conductive material (silicon, silicon carbide, polysilicon, group III/V materials, metal), and plastics (e.g., polyimide-based materials). Of course, the type of transfer substrate used will depend upon the application. Additionally, the transfer substrate can be used to remove the thin film of material from the cleaved substrate after the controlled cleaving process.

A process for fabricating a silicon-on-insulator substrate according to the present invention may be briefly outlined as follows:

(1) Provide a donor silicon wafer (which may be coated with a dielectric material);

(2) Introduce particles into the silicon wafer to a selected depth to define a thickness of silicon film;

(3) Provide a target substrate material (which may be coated with a dielectric material);

(4) Bond the donor silicon wafer to the target substrate material by joining the implanted face to the target substrate material;

(5) Increase global stress (or energy) of implanted region at selected depth without initiating a cleaving action (optional);

(6) Provide stress (or energy) using a fluid jet to a selected region of the bonded substrates to initiate a controlled cleaving action at the selected depth;

(7) Provide additional energy to the bonded substrates to sustain the controlled cleaving action to free the thickness of silicon film from the silicon wafer (optional);

(8) Complete bonding of donor silicon wafer to the target substrate (optional);

(9) Finish surface of cleaved film by etching and hydrogen treatment;

(10) Form epitaxial layer (e.g., silicon, silicon germanium) overlying finished surface; and

(11) Perform remaining steps, if necessary.

The above sequence of steps provides a step of initiating a controlled cleaving action using an energy applied to a selected region(s) of a multi-layered substrate structure to form a cleave front(s) according to the present invention. This initiation step begins a cleaving process in a controlled manner by limiting the amount of energy applied to the substrate. Further propagation of the cleaving action can occur by providing additional energy to selected regions of the substrate to sustain the cleaving action, or using the energy from the initiation step to provide for further propagation of the cleaving action. The steps are also used to finish the cleaved surface using a combination of etch and hydrogen treatment for silicon wafer, for example. This sequence of steps is merely an example and should not limit the scope of the claims defined herein. Further details with regard to the above sequence of steps are described in below in references to the Figs.

Figs. 12-16 are simplified cross-sectional view diagrams of substrates undergoing a fabrication process for a silicon-on-insulator wafer according to the present invention. The process begins by providing a semiconductor substrate similar to the silicon wafer 2100, as shown by Fig. 12. Substrate or donor includes a material region 2101 to be removed, which is a thin relatively uniform film derived from the

substrate material. The silicon wafer includes a top surface 2103, a bottom surface 2105, and a thickness 2107. Material region also includes a thickness (z_0), within the thickness 2107 of the silicon wafer. Optionally, a dielectric layer 2102 (e.g., silicon nitride, silicon oxide, silicon oxynitride) overlies the top surface of the substrate. The present process provides a novel technique for removing the material region 2101 using the following sequence of steps for the fabrication of a silicon-on-insulator wafer.

Selected energetic particles 2109 implant through the top surface of the silicon wafer to a selected depth, which defines the thickness of the material region, termed the thin film of material. As shown, the particles have a desired concentration 2111 at the selected depth (z_0). A variety of techniques can be used to implant the energetic particles into the silicon wafer. These techniques include ion implantation using, for example, beam line ion implantation equipment manufactured from companies such as Applied Materials, Eaton Corporation, Varian, and others. Alternatively, implantation occurs using a plasma immersion ion implantation ("PIII") technique. Furthermore, implantation can occur using ion shower. Of course, techniques used depend upon the application.

Depending upon the application, smaller mass particles are generally selected to reduce a possibility of damage to the material region. That is, smaller mass particles easily travel through the substrate material to the selected depth without substantially damaging the material region that the particles traversed through. For example, the smaller mass particles (or energetic particles) can be almost any charged (e.g., positive or negative) and/or neutral atoms or molecules, or electrons, or the like. In a specific embodiment, the particles can be neutral and/or charged particles including ions of hydrogen and its isotopes, rare gas ions such as helium and its isotopes, and neon. The particles can also be derived from compounds such as gases, e.g., hydrogen gas, water vapor, methane, and other hydrogen compounds, and other light atomic mass particles. Alternatively, the particles can be any combination of the above particles, and/or ions and/or molecular species and/or atomic species.

The process uses a step of joining the implanted silicon wafer to a workpiece or target wafer, as illustrated in Fig. 13. The workpiece may also be a variety of other types of substrates such as those made of a dielectric material (e.g.,

quartz, glass, silicon nitride, silicon dioxide), a conductive material (silicon, polysilicon, group III/V materials, metal), and plastics (e.g., polyimide-based materials). In the present example, however, the workpiece is a silicon wafer.

In a specific embodiment, the silicon wafers are joined or fused together using a low temperature thermal step. The low temperature thermal process generally ensures that the implanted particles do not place excessive stress on the material region, which can produce an uncontrolled cleave action. In one aspect, the low temperature bonding process occurs by a self-bonding process. In particular, one wafer is stripped to remove oxidation therefrom (or one wafer is not oxidized). A cleaning solution treats the surface of the wafer to form O-H bonds on the wafer surface. An example of a solution used to clean the wafer is a mixture of H_2O_2-H_2SO_4. A dryer dries the wafer surfaces to remove any residual liquids or particles from the wafer surfaces. Self-bonding occurs by placing a face of the cleaned wafer against the face of an oxidized wafer.

Alternatively, a self-bonding process occurs by activating one of the wafer surfaces to be bonded by plasma cleaning. In particular, plasma cleaning activates the wafer surface using a plasma derived from gases such as argon, ammonia, neon, water vapor, and oxygen. The activated wafer surface 2203 is placed against a face of the other wafer, which has a coat of oxidation 2205 thereon. The wafers are in a sandwiched structure having exposed wafer faces. A selected amount of pressure is placed on each exposed face of the wafers to self-bond one wafer to the other.

Alternatively, an adhesive disposed on the wafer surfaces is used to bond one wafer onto the other. The adhesive includes an epoxy, polyimide-type materials, and the like. Spin-on-glass layers can be used to bond one wafer surface onto the face of another. These spin-on-glass ("SOG") materials include, among others, siloxanes or silicates, which are often mixed with alcohol-based solvents or the like. SOG can be a desirable material because of the low temperatures (e.g., 150 to 250 Degrees Celsius) often needed to cure the SOG after it is applied to surfaces of the wafers.

Alternatively, a variety of other low temperature techniques can be used to join the donor wafer to the target wafer. For instance, an electro-static bonding technique can be used to join the two wafers together. In particular, one or both wafer

surface(s) is charged to attract to the other wafer surface. Additionally, the donor wafer can be fused to the target wafer using a variety of commonly known techniques. Of course, the technique used depends upon the application.

After bonding the wafers into a sandwiched structure 2300, as shown in Fig. 14, the method includes a controlled cleaving action to remove the substrate material to provide a thin film of substrate material 2101 overlying an insulator 2305 the target silicon wafer 2201. The controlled-cleaving occurs by way of selective energy placement or positioning or targeting 2301, 2303 of energy sources onto the donor and/or target wafers. For instance, an energy impluse(s) can be used to initiate the cleaving action. The impulse (or impulses) is provided using an energy source which include, among others, a mechanical source, a chemical source, a thermal sink or source, and an electrical source.

The controlled cleaving action is initiated by way of any of the previously noted techniques and others and is illustrated by way of Fig. 14. For instance, a process for initiating the controlled cleaving action uses a step of providing energy 2301, 2303 to a selected region of the substrate to initiate a controlled cleaving action at the selected depth (z_0) in the substrate, whereupon the cleaving action is made using a propagating cleave front to free a portion of the substrate material to be removed from the substrate. In a specific embodiment, the method uses a single impulse to begin the cleaving action, as previously noted. Alternatively, the method uses an initiation impulse, which is followed by another impulse or successive impulses to selected regions of the substrate. Alternatively, the method provides an impulse to initiate a cleaving action which is sustained by a scanned energy along the substrate. Alternatively, energy can be scanned across selected regions of the substrate to initiate and/or sustain the controlled cleaving action.

Optionally, an energy or stress of the substrate material is increased toward an energy level necessary to initiate the cleaving action, but not enough to initiate the cleaving action before directing an impulse or multiple successive impulses to the substrate according to the present invention. The global energy state of the substrate can be raised or lowered using a variety of sources such as chemical, mechanical, thermal (sink or source), or electrical, alone or in combination. The

chemical source can include particles, fluids, gases, or liquids. These sources can also include chemical reaction to increase stress in the material region. The chemical source is introduced as flood, time-varying, spatially varying, or continuous. In other embodiments, a mechanical source is derived from rotational, translational, compressional, expansional, or ultrasonic energies. The mechanical source can be introduced as flood, time-varying, spatially varying, or continuous. In further embodiments, the electrical source is selected from an applied voltage or an applied electro-magnetic field, which is introduced as flood, time-varying, spatially varying, or continuous. In still further embodiments, the thermal source or sink is selected from radiation, convection, or conduction. This thermal source can be selected from, among others, a photon beam, a fluid jet, a liquid jet, a gas jet, an electro/magnetic field, an electron beam, a thermo-electric heating, and a furnace. The thermal sink can be selected from a fluid jet, a liquid jet, a gas jet, a cryogenic fluid, a super-cooled liquid, a thermo-electric cooling means, an electro/magnetic field, and others. Similar to the previous embodiments, the thermal source is applied as flood, time-varying, spatially varying, or continuous. Still further, any of the above embodiments can be combined or even separated, depending upon the application. Of course, the type of source used depends upon the application. As noted, the global source increases a level of energy or stress in the material region without initiating a cleaving action in the material region before providing energy to initiate the controlled cleaving action.

In a preferred embodiment, the method maintains a temperature which is below a temperature of introducing the particles into the substrate. In some embodiments, the substrate temperature is maintained between -200 and 450 Degrees Celsius during the step of introducing energy to initiate propagation of the cleaving action. Substrate temperature can also be maintained at a temperature below 400 or below 350 Degrees Celsius. In preferred embodiments, the method uses a thermal sink to initiate and maintain the cleaving action, which occurs at conditions significantly below room temperature.

In an alternative preferred embodiment, the mechanical and/or thermal source can be a fluid jet that is pressurized (e.g., compressional) according to an embodiment of the present invention. The fluid jet (or liquid jet or gas jet) impinges on

an edge region of substrate 2300 to initiate the controlled cleaving process. The fluid jet from a compressed or pressurized fluid source is directed to a region at the selected depth 2111 to cleave a thickness of material region 2101 from substrate 2100. The fluid jet separates region 2101 from substrate 2100 that separate from each other at selected depth 2111. The fluid jet can be adjusted to initiate and maintain the controlled cleaving process to separate material 2101 from substrate 2100. Depending upon the application, the fluid jet can be adjusted in direction, location, and magnitude to achieve the desired controlled cleaving process.

A final bonding step occurs between the target wafer and thin film of material region according to some embodiments, as illustrated by Fig. 15. In one embodiment, one silicon wafer has an overlying layer of silicon dioxide, which is thermally grown overlying the face before cleaning the thin film of material. The silicon dioxide can also be formed using a variety of other techniques, e.g., chemical vapor deposition. The silicon dioxide between the wafer surfaces fuses together thermally in this process.

In some embodiments, the oxidized silicon surface from either the target wafer or the thin film of material region (from the donor wafer) are further pressed together and are subjected to an oxidizing ambient 2401. The oxidizing ambient can be in a diffusion furnace for steam oxidation, hydrogen oxidation, or the like. A combination of the pressure and the oxidizing ambient fuses the two silicon wafers together at the oxide surface or interface 2305. These embodiments often require high temperatures (e.g., 700 Degrees Celsius).

Alternatively, the two silicon surfaces are further pressed together and subjected to an applied voltage between the two wafers. The applied voltage raises temperature of the wafers to induce a bonding between the wafers. This technique limits the amount of crystal defects introduced into the silicon wafers during the bonding process, since substantially no mechanical force is needed to initiate the bonding action between the wafers. Of course, the technique used depends upon the application.

After bonding the wafers, silicon-on-insulator has a target substrate with an overlying film of silicon material and a sandwiched oxide layer between the target

substrate and the silicon film, as also illustrated in Fig. 15. The detached surface of the film of silicon material is often rough 2404 and needs finishing. The rough surface for silicon wafers is often about two to eight nanometers RMS or greater. This roughness often should be removed before further processing. In a specific embodiment, the detached surface has a concentration of hydrogen bearing particles therein and thereon from the previous implanting step.

To smooth or treat surface 2404, the substrate is subjected to thermal treatment 2401 in a hydrogen bearing environment. Additionally, the substrate is also subjected to an etchant including a halogen bearing compound such as HCl, HBr, HI, HF, and others. The etchant can also be a fluorine bearing compound such as SF_6, C_xF_x.

In preferred embodiments, the present substrate undergoes treatment using a combination of etchant and thermal treatment in a hydrogen bearing environment. In a specific embodiment, the etchant is HCl gas or the like. The thermal treatment uses a hydrogen etchant gas. In some embodiments, the etchant gas is a halogenated gas, e.g., HCl, HF, HI, HBr, SF_6, CF_4, NF_3, and CCl_2F_2. The etchant gas can also be mixed with another halogen gas, e.g., chlorine, fluorine. The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be from an epitaxial chamber, which has lamps for rapidly heating a substrate. In an embodiment using a silicon wafer and hydrogen gas, the tool can heat the substrate at a rate of about 10 Degrees Celsius and greater or 20 Degrees Celsius and greater, depending upon the embodiment.

In one embodiment, it is believed that the hydrogen particles in the detached surface improves the surface smoothing process. Here, the hydrogen particles have been maintained at a temperature where they have not diffused out of the substrate. In a specific embodiment, the concentration of hydrogen particles ranges from about 10^{21} to about 5×10^{22} atoms/cm^3. Alternatively, the concentration of hydrogen particles is at least about 6×10^{21} atoms/cm^3. Depending upon the embodiment, the particular concentration of the hydrogen particles can be adjusted.

Still further in other embodiments, the present substrate undergoes a process of hydrogen treatment or implantation before thermal treatment. Here, the

substrate, including the detached film, is subjected to hydrogen bearing particles by way of implantation, diffusion, or any combination thereof. In some embodiments, where hydrogen has diffused out from the initial implant, a subsequent hydrogen treatment process can occur to increase a concentration of hydrogen in the detached film. The present hydrogen treatment process can occur for substrates made by way of the controlled cleaving process, Smart Cut™, and others, which may form an uneven or rough surface finish after detachment. A finished wafer after smoothing or surface treatment is shown in Fig. 16. Here, the finished wafer includes a substantially smooth surface 2601, which is generally good enough for the manufacture of integrated circuits without substantial polishing or the like.

Moreover, the present technique for finishing the cleaved surface can use a combination of etchant, deposition, and thermal treatment to smooth the cleaved film. Here, the cleaved film is subjected to hydrogen bearing compounds such as HCl, HBr, HI, HF, and others. Additionally, the cleaved film is subjected to for example, deposition, during a time that the film is subjected to the hydrogen bearing compounds, which etch portions of the cleaved film. Using a silicon cleaved film for example, the deposition may occur by way of a silicon bearing compound such as silanes, e.g., $Si_xCl_yH_z$,, SiH_4, $SiCl_x$, and other silicon compounds. Accordingly, the present method subjects the cleaved film to a combination of etching and deposition using a hydrogen bearing compound and a silicon bearing compound. Additionally, the cleaved surface undergoes thermal treatment while being subjected to the combination of etchant and deposition gases The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be from an epitaxial chamber, which has lamps for rapidly heating a substrate. In an embodiment using a silicon wafer and hydrogen gas, the tool can heat the substrate at a rate of about 10 Degrees Celsius/second and greater or 20 Degrees Celsius/second and greater, depending upon the embodiment. In some embodiments, the process is also maintained at about 1 atmosphere, but is not limited to this pressure.

In a specific embodiment, the silicon-on-insulator substrate undergoes a series of process steps for formation of integrated circuits thereon. These processing

steps are described in S. Wolf, Silicon Processing for the VLSI Era (Volume 2), Lattice Press (1990), which is hereby incorporated by reference for all purposes.

Although the above description is in terms of a silicon wafer, other substrates may also be used. For example, the substrate can be almost any monocrystalline, polycrystalline, or even amorphous type substrate. Additionally, the substrate can be made of III/V materials such as gallium arsenide, gallium nitride (GaN), and others. The multi-layered substrate can also be used according to the present invention. The multi-layered substrate includes a silicon-on-insulator substrate, a variety of sandwiched layers on a semiconductor substrate, and numerous other types of substrates. Additionally, the embodiments above were generally in terms of providing a pulse of energy to initiate a controlled cleaving action. The pulse can be replaced by energy that is scanned across a selected region of the substrate to initiate the controlled cleaving action. Energy can also be scanned across selected regions of the substrate to sustain or maintain the controlled cleaving action. One of ordinary skill in the art would easily recognize a variety of alternatives, modifications, and variations, which can be used according to the present invention.

SMOOTHING METHOD USING A RELEASE LAYER

According to another embodiment of the present invention, as shown in Fig. 17A, a silicon single-crystal substrate 2821 is first prepared and then rendered porous at its surface layer. Numeral 2822 denotes the resulting porous layer. As shown in Fig. 17B, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layer 2822. Then, a porous layer (ion-implanted layer) 2823 having large porosity is formed in the porous layer 2822. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1 \times 10^{14}/cm^2$ and more preferably $1 \times 10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed or at least one of compressive, tensile and shear stresses is applied to the

wafer in a direction perpendicular to the surface as necessary, so as to divide the semiconductor substrate into two at the ion-implanted layer as a border. In the case of the heat treatment atmosphere being an oxidizing atmosphere, the pore walls are oxidized so that attention should be given to preventing the silicon region from being all changed into silicon oxide due to over oxidation.

In Fig. 17C, the extremely thin porous substrate obtained by the present invention is shown. Since the division of the substrate starts spontaneously upon the heat treatment or the like as a trigger due to the internal stress introduced upon the implantation, the extremely thin porous structure can be formed uniformly all over the substrate. The pores of the porous structure are formed from one main surface of the substrate toward the other main surface. Accordingly, when the gas is implanted under pressure from the one main surface, it is ejected out from the other main surface. In this case, since the pore size of the porous structure is in the range from several nanometers to several tens of nanometers, a particle greater than this can not pass therethrough. On the other hand, although pressure loss is caused depending on the pore size, the pore density and a thickness of the extremely thin porous substrate, the strength of the substrate and the pressure loss can be both within the practical range if the thickness of the porous layer is approximately no more than 20 microns.

As shown in Fig. 17D, porous layer 2822, which has an overlying layer 2823, is subjected to further processing. Here, layer 2823 is removed by etching techniques. Once layer 2823 is removed, a surface treatment process 2824 is provided. The surface treatment process removes surface roughness from the surface 2825 of the porous layer. The film of silicon material is often rough 2825 and needs finishing. The rough surface for silicon wafers is often about two to eight nanometers RMS or greater. This roughness often should be removed before further processing. In a specific embodiment, the detached surface has a concentration of hydrogen bearing particles therein and thereon from the previous implanting step.

To smooth or treat the surface, the substrate is subjected to thermal treatment in a hydrogen bearing environment. Additionally, the substrate is also subjected to an etchant including a halogen bearing compound such as HCl, HBr, HI, HF, and others. The etchant can also be a fluorine bearing compound such as SF_6,

C_xF_x. In preferred embodiments, the present substrate undergoes treatment using a combination of etchant and thermal treatment in a hydrogen bearing environment. In a specific embodiment, the etchant is HCl gas or the like. The thermal treatment uses a hydrogen etchant gas. In some embodiments, the etchant gas is a halogenated gas, e.g., HCl, HF, HI, HBr, SF_6, CF_4, NF_3, and CCl_2F_2. The etchant gas can also be mixed with another halogen gas, e.g., chlorine, fluorine. The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be an epitaxial chamber, which has lamps for rapidly heating a substrate. In an embodiment using a silicon wafer and hydrogen gas, the tool can heat the substrate at a rate of about 10 Degrees Celsius/second and greater or 20 Degrees Celsius/second and greater, depending upon the embodiment.

In one embodiment, it is believed that the hydrogen particles in the detached surface improves the surface smoothing process. Here, the hydrogen particles have been maintained at a temperature where they have not diffused out of the substrate. In a specific embodiment, the concentration of hydrogen particles ranges from about 10^{21} to about 5 X 10^{22} atoms/cm^3. Alternatively, the concentration of hydrogen particles is at least about 6 X 10^{21} atoms/cm^3. Depending upon the embodiment, the particular concentration of the hydrogen particles can be adjusted.

Still further in other embodiments, the present substrate undergoes a process of hydrogen treatment or implantation before thermal treatment purposes. Here, the substrate, including the detached film, is subjected to hydrogen bearing particles by way of implantation, diffusion, or any combination thereof. In some embodiments, where hydrogen has diffused out from the initial implant, a subsequent hydrogen treatment process can occur to increase a concentration of hydrogen in the detached film. The present hydrogen treatment process can occur for substrates made by way of other processes such as those noted below.

Moreover, the present technique for finishing the cleaved surface can use a combination of etchant, deposition, and thermal treatment to smooth the cleaved film. Here, the cleaved film is subjected to hydrogen bearing compounds such as HCl, HBr, HI, HF, and others. Additionally, the cleaved film is subjected to for example, deposition, during a time that the film is subjected to the hydrogen bearing compounds,

which etch portions of the cleaved film. Using a silicon cleaved film for example, the deposition may occur by way of a silicon bearing compound such as silanes, e.g., $Si_xCl_yH_z$, SiH_4, $SiCl_x$, and other silicon compounds. Accordingly, the present method subjects the cleaved film to a combination of etching and deposition using a hydrogen bearing compound and a silicon bearing compound. Additionally, the cleaved surface undergoes thermal treatment while being subjected to the combination of etchant and deposition gases. The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be an epitaxial chamber, which has lamps for rapidly heating a substrate. In an embodiment using a silicon wafer and hydrogen gas, the tool can heat the substrate at a rate of about 10 Degrees Celsius/second and greater or 20 Degrees Celsius/second and greater, depending upon the embodiment.

As shown in Fig. 18A, a silicon single-crystal substrate 2841 is first prepared and then rendered porous at its surface layer. Numeral 2842 denotes the resulting porous layer. Subsequently, as shown in Fig. 18B, at least one non-porous thin film 2843 is formed on the porous layer. The film to be formed is arbitrarily selected from among a single-crystal silicon film, a polycrystalline silicon film, an amorphous silicon film, a metal film, a compound semiconductor film, a superconductive film and the like. An element structure such as a MOSFET may be formed using the film.

As shown in Fig. 18C, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layer 2842 so as to form an implanted layer 2844. When observing the implanted layer by a transmission electron microscope, formation of numberless micro-cavities can be seen. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1 \times 10^{14}/cm^2$ and more preferably $1 \times 10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed as necessary. In case of the heat treatment atmosphere being the oxidizing

atmosphere, the pore walls are oxidized so that attention should be given to preventing the silicon region from being all changed into silicon oxide due to over oxidation.

As shown in Fig. 18D, after abutting a support substrate 2845 and the surface of the first substrate with each other at room temperature, they are bonded to each other through anodic bonding, pressurization, heat treatment or a combination thereof. As a result, both substrates are firmly coupled with each other.

When single-crystal silicon is deposited, it is preferable to perform the bonding after oxidized silicon is formed on the surface of single-crystal silicon through thermal oxidation or the like. On the other hand, the support substrate can be selected from among a silicon substrate, a silicon substrate with a silicon oxide film formed thereon, a light transmittable substrate such as quartz, a sapphire substrate and the like, but not limited thereto as long as the surface serving for the bonding is fully flat. The bonding may be performed in three plies with an insulating thin plate interposed therebetween.

Subsequently, the substrates are divided at the ion-implanted layer 2844 in the porous silicon layer 2842 (Fig. 18E). The structure of the second substrate side includes the porous silicon layer 2842, the non-porous thin film (for example, the single-crystal silicon layer) 2843 and the second substrate 2845.

Further, the porous silicon layer 2842 is selectively removed. In case of the non-porous thin film being single-crystal silicon, only the porous silicon layer 2842 is subjected to the electroless wet chemical etching using at least one of the normal silicon etching liquid, hydrofluoric acid being the porous silicon selective etching liquid, a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide water to hydrofluoric acid, buffered hydrofluoric acid, and a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide to buffered hydrofluoric acid, so as to render the film formed in advance on the porous layer of the first substrate remain on the second substrate. As described above in detail, only the porous silicon layer can be selectively etched using the normal silicon etching liquid due to the extensive surface area of porous silicon. Alternatively, the porous silicon layer 2842 may be removed through selective polishing using the single-crystal silicon layer 2843 as a polishing stopper.

In the case where the compound semiconductor layer is formed on the porous layer, only the porous silicon layer 2842 is subjected to chemical etching using the etching liquid which has the greater etching speed for silicon relative to the compound semiconductor, so that the thickness-reduced single-crystal compound semiconductor layer 2843 remains on the insulating substrate 2845. Alternatively, the porous silicon layer 2842 is removed through selective polishing using the single-crystal compound semiconductor layer 2843 as a polishing stopper.

In Fig. 18F, the semiconductor substrate of the present invention is shown. On the insulating substrate 2845, the non-porous thin film, such as the single-crystal silicon thin film 2843, is formed in a large area all over the wafer, flatly and uniformly reduced in thickness. The semiconductor substrate thus obtained can be suitably used in production of an insulated electronic element.

The silicon single-crystal substrate 2841 can be reused as an silicon single-crystal substrate 2841 after removing remaining any porous silicon and after performing surface-flattening if the surface flatness makes the substrate unusable. Alternatively, a non-porous thin film may be again formed without removing porous silicon so as to provide the substrate as shown in Fig. 18B, which is then subjected to the processes shown in Figs. 18C to 18F. In embodiments where flattening is desirable, a novel surface processing step is provided, as shown in Fig. 18G. Alternatively, smoothing or flattening of the single crystal silicon thin film is also provided, as shown in Fig. 18G.

Fig. 18G illustrates a surface 2847 smoothing step for either surface 2846A or 2846B according to an embodiment of the present invention. As show, surface 2847 is often rough and needs finishing. The present surface treatment process removes surface roughness from the surface 2847 of the porous layer. The rough surface for silicon wafers is often about two to eight nanometers RMS or greater. This roughness often should be removed before further processing. In a specific embodiment, the detached surface has a concentration of hydrogen bearing particles therein and thereon from the previous implanting step.

To smooth or treat the surface, the substrate is subjected to thermal treatment in a hydrogen bearing environment. Additionally, the substrate is also

subjected to an etchant including a halogen bearing compound such as HCl, HBr, HI, HF, and others. The etchant can also be a fluorine bearing compound such as SF_6, C_xF_x. In preferred embodiments, the present substrate undergoes treatment using a combination of etchant and thermal treatment in a hydrogen bearing environment. In a specific embodiment, the etchant is HCl gas or the like. The thermal treatment uses a hydrogen etchant gas. In some embodiments, the etchant gas is a halogenated gas, e.g., HCl, HF, HI, HBr, SF_6, CF_4, NF_3, and CCl_2F_2.. The etchant gas can also be mixed with another halogen gas, e.g., chlorine, fluorine. The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be from an epitaxial chamber, which has lamps for rapidly heating a substrate. In an embodiment using a silicon wafer and hydrogen gas, the tool can heat the substrate at a rate of about 10 Degrees Celsius/second and greater or 20 Degrees Celsius/second and greater, depending upon the embodiment.

In one embodiment, it is believed that the hydrogen particles in the detached surface improves the surface smoothing process. Here, the hydrogen particles have been maintained at a temperature where they have not diffused out of the substrate. In a specific embodiment, the concentration of hydrogen particles ranges from about 10^{21} to about 5 X 10^{22} atoms/cm^3. Alternatively, the concentration of hydrogen particles is at least about 6 X 10^{21} atoms/cm^3. Depending upon the embodiment, the particular concentration of the hydrogen particles can be adjusted.

Still further in other embodiments, the present substrate undergoes a process of hydrogen treatment or implantation before thermal treatment purposes. Here, the substrate, including the detached film, is subjected to hydrogen bearing particles by way of implantation, diffusion, or any combination thereof. In some embodiments, where hydrogen has diffused out from the initial implant, a subsequent hydrogen treatment process can occur to increase a concentration of hydrogen in the detached film. The present hydrogen treatment process can occur for substrates made by way of other processes such as those noted below.

Moreover, the present technique for finishing the cleaved surface can use a combination of etchant, deposition, and thermal treatment to smooth the cleaved film. Here, the cleaved film is subjected to hydrogen bearing compounds such as HCl, HBr,

HI, HF, and others. Additionally, the cleaved film is subjected to for example, deposition, during a time that the film is subjected to the hydrogen bearing compounds, which etch portions of the cleaved film. Using a silicon cleaved film for example, the deposition may occur by way of a silicon bearing compound such as silanes, e.g., $Si_xCl_yH_z$, SiH_4, $SiCl_x$, and other silicon compounds. Accordingly, the present method subjects the cleaved film to a combination of etching and deposition using a hydrogen bearing compound and a silicon bearing compound. Additionally, the cleaved surface undergoes thermal treatment while being subjected to the combination of etchant and deposition gases. The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be an epitaxial chamber, which has lamps for rapidly heating a substrate. In an embodiment using a silicon wafer and hydrogen gas, the tool can heat the substrate at a rate of about 10 Degrees Celsius/second and greater or 20 Degrees Celsius/second and greater, depending upon the embodiment.

As shown in Fig. 19A, a silicon single-crystal substrate 2851 is first prepared and then rendered porous at both surface layers thereof. Numerals 2852 and 2853 denote the obtained porous layers. Subsequently, as shown in Fig. 19B, at least one non-porous thin film 2854, 2855 is formed on each of the porous layers. The film to be formed is arbitrarily selected from among a single-crystal silicon film, a polycrystalline silicon film, an amorphous silicon film, a metal film, a compound semiconductor film, a superconductive film and the like. An element structure such as a MOSFET may be formed from the film.

As shown in Fig. 19C, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layers 2852 and 2853 so as to form implanted layers 2856 and 2857. When observing the implanted layers by a transmission electron microscope, formation of numberless micro-cavities can be seen, and accordingly the porosity enlarges. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but they are approximately no less than $1 \times 10^{14}/cm^2$ and more preferably $1 \times 10^{15}/cm^2$. When

setting the projection range deeper, channeling ion implantation may be employed. After the implantation, heat treatment is performed as necessary. In the case of the heat treatment atmosphere being oxidizing atmosphere, the pore walls are oxidized so that attention should be given to preventing the silicon region from being all changed into silicon oxide due to over oxidation.

As shown in Fig. 19D, after abutting two support substrates 2858 and 2859 and the surfaces of the non-porous thin films 2854 and 2855 of the first substrate with each other at room temperature, they are bonded to each other through anode bonding, pressurization, heat treatment or a combination thereof. As a result, the three substrates are firmly coupled with each other. Alternatively, the bonding may be performed in five plies with insulating thin plates interposed therebetween.

When single-crystal silicon is deposited, it is preferable to perform the bonding after oxidized silicon is formed on the surface of single-crystal silicon through thermal oxidation or the like. On the other hand, the support substrate can be selected from among a silicon substrate, a silicon substrate with a silicon oxide film formed thereon, a light transmittable substrate such as quartz, a sapphire substrate and the like, but not limited thereto as long as the surface serving for the bonding is completely flat. The bonding may be performed in three plies with an insulating thin plate interposed therebetween.

Subsequently, the substrates are divided at the ion-implanted layers 2856 and 2857 in the porous silicon layers 2852 and 2853 (Fig. 19E). The structure of each of the two support substrate sides includes the porous silicon layer 2852, 2853, the non-porous thin film (for example, the single-crystal silicon layer) 2854, 2855 and the support substrate 2858, 2859.

Further, the porous silicon layer 2852, 2853 is selectively removed. In case of the non-porous thin film being single-crystal silicon, only the porous silicon layer 2852, 2853 is subjected to the electroless wet chemical etching using at least one of the normal silicon etching liquid, hydrofluoric acid being the porous silicon selective etching liquid, a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide to hydrofluoric acid, buffered hydrofluoric acid, and a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide to buffered

hydrofluoric acid, so that the film formed in advance on the porous layer of the first substrate remains on the support substrate. As described above in detail, only the porous silicon layer can be selectively etched using the normal silicon etching liquid due to the extensive surface area of porous silicon. Alternatively, the porous silicon layer 2852, 2853 may be removed through selective polishing using the single-crystal silicon layer 2854, 2855 as a polishing stopper.

In the case where the compound semiconductor layer is formed on the porous layer, only the porous silicon layer 2852, 2853 is subjected to chemical etching using the etching liquid which has the greater etching speed for silicon relative to the compound semiconductor, so that the thickness-reduced single-crystal compound semiconductor layer 2854, 2855 remains on the insulating substrate. Alternatively, the porous silicon layer 2852, 2853 is removed through selective polishing using the single-crystal compound semiconductor layer 2854, 2855 as a polishing stopper.

In Fig. 19F, the semiconductor substrates of the present invention are shown. On the support substrates, the non-porous thin films, such as the single-crystal silicon thin films 2854 and 2855, are formed in large area all over the wafer, flatly and uniformly reduced in thickness, so that the two semiconductor substrates are simultaneously formed. The semiconductor substrates thus obtained can be suitably used also in view of production of the insulated electronic elements.

The first silicon single-crystal substrate 2851 can be reused as a first silicon single-crystal substrate 2851 after removing remaining porous silicon and after performing surface-flattening if the surface flatness makes it unusable. Alternatively, a non-porous thin film may be again formed without removing porous silicon so as to provide the substrate as shown in Fig. 19B, which is then subjected to the processes shown in Figs. 19C to 19F. The support substrates 58 and 59 are not necessarily identical with each other.

In a specific embodiment, any of the above surfaces can be treated to for smoothing purposes. Here, the final silicon surface may often be rough and needs finishing. The present surface treatment process removes surface roughness from the surface of the porous layer or silicon material. The film of silicon material is often rough and needs finishing. The rough surface for silicon wafers is often about two to

eight nanometers RMS or greater. This roughness often should be removed before further processing. In a specific embodiment, the detached surface has a concentration of hydrogen bearing particles therein and thereon from the previous implanting step.

To smooth or treat the surface, the substrate is subjected to thermal treatment in a hydrogen bearing environment. Additionally, the substrate is also subjected to an etchant including a halogen bearing compound such as HCl, HBr, HI, HF, and others. The etchant can also be a fluorine bearing compound such as SF_6, C_xF_x. In preferred embodiments, the present substrate undergoes treatment using a combination of etchant and thermal treatment in a hydrogen bearing environment. In a specific embodiment, the etchant is HCl gas or the like. The thermal treatment uses a hydrogen etchant gas. In some embodiments, the etchant gas is a halogenated gas, e.g., HCl, HF, HI, HBr, SF_6, CF_4, NF_3, and CCl_2F_2. The etchant gas can also be mixed with another halogen gas, e.g., chlorine, fluorine. The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be an epitaxial chamber, which has lamps for rapidly heating a substrate. In an embodiment using a silicon wafer and hydrogen gas, the tool can heat the substrate at a rate of about 10 Degrees Celsius/second and greater or 20 Degrees Celsius/second and greater, depending upon the embodiment.

In one embodiment, it is believed that the hydrogen particles in the detached surface improves the surface smoothing process. Here, the hydrogen particles have been maintained at a temperature where they have not diffused out of the substrate. In a specific embodiment, the concentration of hydrogen particles ranges from about 10^{21} to about 5×10^{22} atoms/cm^3. Alternatively, the concentration of hydrogen particles is at least about 6×10^{21} atoms/cm^3. Depending upon the embodiment, the particular concentration of the hydrogen particles can be adjusted.

Still further in other embodiments, the present substrate undergoes a process of hydrogen treatment or implantation before thermal treatment purposes. Here, the substrate, including the detached film, is subjected to hydrogen bearing particles by way of implantation, diffusion, or any combination thereof. In some embodiments, where hydrogen has diffused out from the initial implant, a subsequent hydrogen treatment process can occur to increase a concentration of hydrogen in the

detached film. The present hydrogen treatment process can occur for substrates made by way of other processes such as those noted below.

Moreover, the present technique for finishing the cleaved surface can use a combination of etchant, deposition, and thermal treatment to smooth the cleaved film. Here, the cleaved film is subjected to hydrogen bearing compounds such as HCl, HBr, HI, HF, and others. Additionally, the cleaved film is subjected to for example, deposition, during a time that the film is subjected to the hydrogen bearing compounds, which etch portions of the cleaved film. Using a silicon cleaved film for example, the deposition may occur by way of a silicon bearing compound such as silanes, e.g., $Si_xCl_yH_z$, SiH_4, $SiCl_x$, and other silicon compounds. Accordingly, the present method subjects the cleaved film to a combination of etching and deposition using a hydrogen bearing compound and a silicon bearing compound. Additionally, the cleaved surface undergoes thermal treatment while being subjected to the combination of etchant and deposition gases The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be an epitaxial chamber, which has lamps for rapidly heating a substrate. In an embodiment using a silicon wafer and hydrogen gas, the tool can heat the substrate at a rate of about 10 Degrees Celsius/second and greater or 20 Degrees Celsius/second and greater, depending upon the embodiment.

An alternative embodiment will be described with reference to Figs. 20A to 20E. First, a single-crystal silicon substrate 2900 is anodized to form a porous silicon layer 2901 (Fig. 20A). In this case, a thickness to be rendered porous is in the range from several micrometers to several tens of micrometers on one surface layer of the substrate. It may be arranged to anodize the whole silicon substrate 2900.

The method of forming porous silicon will be explained using Figs. 23A and 23B. First, as the substrate, a p-type single-crystal silicon substrate 3600 is prepared. An n-type may also be used. However, in this case, it is necessary that the substrate is limited to a low-resistance substrate or that the light is applied onto the surface of the substrate so as to facilitate generation of the holes. The substrate 3600 is set in an apparatus as shown in Fig. 23A. Specifically, one side of the substrate is in contact with a hydrofluoric acid solution 3604 having therein a negative electrode 3606,

while the other side of the substrate is in contact with a positive metal electrode 3605. On the other hand, as shown in Fig. 23B, a positive electrode 3605' may also be provided in a solution 3604'. In any case, the substrate is first rendered porous from the negative electrode side abutting the hydrofluoric acid solution. As the hydrofluoric acid solution 3604, concentrated hydrofluoric acid (49% HF) is used in general. As diluted by pure water (H_2O), although depending on current values, etching occurs from a certain concentration so that it is not preferable. During anodization, bubbles are generated from the surface of the substrate 3600. Alcohol may be added as a surface active agent for effective removal of the bubbles. As alcohol, methanol, ethanol, propanol, isopropanol or the like is used. Instead of the surface active agent, an agitator may be used to agitate the solution to achieve anodization. The negative electrode 3606 is made of a material, such as gold (Au) or platinum (Pt), which does not corrode relative to the hydrofluoric acid solution. A material of the positive electrode 3605 may be metal which is used in general. On the other hand, since the hydrofluoric acid solution 3604 reaches the positive electrode 3605 when anodization is achieved relative to the whole substrate 3600, it is preferable to coat the surface of the positive electrode 3605 with a metal film which is resistive to the hydrofluoric acid solution. The maximum current value for anodization is several hundreds of mA/cm^2, while the minimum current value therefor is arbitrary, other than zero. This current value is determined in range where the good-quality epitaxial growth is achieved on the surface of porous silicon. In general, as the current value increases, the anodization speed increases and the density of the porous silicon layer decreases. That is, the volume of the pores increases. This changes the condition of the epitaxial growth.

On the porous layer 2901 thus formed, a non-porous single-crystal silicon layer 2902 is epitaxially-grown (Fig. 20B). Subsequently, the surface of the epitaxial layer 2902 is oxidized (including thermal oxidation) so as to form an SiO_2 layer 2903 (Fig. 20C). This is necessary because, if the epitaxial layer is directly bonded to the support substrate in the next process, impurities tend to segregate at the bonded interface and dangling bonds of atoms at the interface increase, which will cause the thin film device to be unusable. However, this process is not essential, but may be omitted in a device structure wherein such phenomena are not serious. The SiO_2 layer

2903 works as an insulating layer of the SOI substrate and should be formed on at least one side of the substrate to be bonded. There are various ways to form of the insulating layer.

Upon oxidation, a thickness of the oxidized film is set to a value which is free of contamination taken into the bonded interface from the atmosphere.

Thereafter, the foregoing ion implantation is performed to form a layer with large porosity in the porous silicon layer 2901. The substrate 2900 having the foregoing epitaxial surface with the oxidized surface and a support substrate 2910 having an SiO_2 layer 2904 on the surface are prepared. The support substrate 2910 may be a silicon substrate whose surface is oxidized (including thermal oxidation), quartz glass, crystallized glass, an arbitrary substrate with SiO_2 deposited thereon, or the like. A silicon substrate without the SiO_2 layer 2904 may also be used as the support substrate.

The foregoing two substrates are bonded together after cleaning them (Fig. 20D). The cleaning is performed pursuant to the process of cleaning (for example, before oxidation) the normal semiconductor substrate. By pressurizing the whole substrate after the bonding, the bonding strength can be enhanced.

Subsequently, the bonded substrates are subjected to heat treatment. Although the higher temperature is preferable for the heat treatment, if it is too high, the porous layer 2901 tends to cause structural change or the impurities contained in the substrate tend to be diffused into the epitaxial layer. Thus, it is necessary to select temperature and time which does not cause these problems. Specifically, about 600 to 1,100° C is preferable. On the other hand, there is such are substrates that can not be subjected to thermal treatment at the high temperature. For example, in case of the support substrate 2910 being made of quartz glass, it can be subjected to the thermal treatment only at the temperature no greater than 200° C due to differences in the thermal expansion coefficients between silicon and quartz. If this temperature is exceeded, the bonded substrates may be separated or ruptured due to stress. The thermal treatment is sufficient as long as it can endure the stress upon grinding or etching of the bulk silicon 2900 performed in the next process. Accordingly, even at

the temperature no greater than 200° C, the process can be performed by optimizing the surface processing condition for activation.

Then, by the foregoing method, the substrates are separated into two at the porous silicon layer having the large porosity. The layer having the large porosity can be formed by altering current in the anodization, besides the ion implantation. Subsequently, the silicon substrate portion 2900 and the porous portion 2901 are selectively removed with the epitaxial layer 2902 remaining (Fig. 20E). In this fashion, the SOI substrate is obtained.

The following processes may be added to the foregoing processes:

(1) The thickness of the wall between the adjacent holes in the oxidized (preoxidation) porous silicon layer, i.e., the pore internal walls of the porous layer, is very small, that is, several nanometers to several tens of nanometers. Thus, if the high-temperature process is applied to the porous layer upon formation of the epitaxial silicon layer or upon heat treatment after bonding, the pore wall may agglomerate and enlarge so that the pore wall may clog the pore and lower the etching speed. In view of this, after formation of the porous layer, a thin oxidized film is formed on the pore wall so as to suppress the enlargement of the pore wall. On the other hand, since it is necessary to epitaxially-grow the non-porous single-crystal silicon layer on the porous layer, it is necessary to oxidize only the surface of the pore inner wall such that the monocrystalline property remains inside the pore wall of the porous layer. It is preferable that the oxidized film is in the range of several angstroms to several tens of angstroms. The oxidized film of such a thickness is formed through heat treatment in an oxygen atmosphere at the temperature of 200° C to 700° C, and more preferably 250° C to 500° C.

(2) Thermal Treatment and Etching

In a specific embodiment, the present invention includes a method of applying a thermal treatment and etching to the surface or surfaces of the substrate for smoothing purposes. Here, small roughness on the silicon surface can be removed to obtain very smooth silicon surface. The combination of at least thermal treatment and etching can be performed, for example, after formation of the porous silicon layer and before formation of the epitaxial silicon layer. Apart from this, the thermal treatment

and etching can be performed to the SOI substrate obtained after etching removal of the porous silicon layer. Through the thermal treatment and etching process performed before formation of the epitaxial silicon layer, a phenomenon that the pore surface is closed due to migration of silicon atoms forming the porous silicon surface. When the epitaxial silicon layer is formed in the state where the pore surface is closed, the epitaxial silicon layer with fewer crystal defects can be achieved. On the other hand, through the thermal treatment and etching process performed after etching of the porous silicon layer, the epitaxial silicon surface which was more or less roughened by etching can be smoothed out, and boron from the clean room inevitably taken into the bonded interface upon bonding and boron thermally diffused in the epitaxial silicon layer from the porous silicon layer can be removed.

As previously noted, to smooth or treat the surface, the substrate is subjected to thermal treatment in a hydrogen bearing environment. Additionally, the substrate is also subjected to an etchant including a halogen bearing compound such as HCl, HBr, HI, HF, and others. The etchant can also be a fluorine bearing compound such as SF_6, C_xF_x. In preferred embodiments, the present substrate undergoes treatment using a combination of etchant and thermal treatment in a hydrogen bearing environment. In a specific embodiment, the etchant is HCl gas or the like. The thermal treatment uses a hydrogen etchant gas. In some embodiments, the etchant gas is a halogenated gas, e.g., HCl, HF, HI, HBr, SF_6, CF_4, NF_3, and CCl_2F_2. The etchant gas can also be mixed with another halogen gas, e.g., chlorine, fluorine. The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be from an epitaxial chamber, which has lamps for rapidly heating a substrate. In an embodiment using a silicon wafer and hydrogen gas, the tool can heat the substrate at a rate of about 10 Degrees Celsius/second and greater or 20 Degrees Celsius/second and greater, depending upon the embodiment.

In one embodiment, it is believed that the hydrogen particles in the detached surface improves the surface smoothing process. Here, the hydrogen particles have been maintained at a temperature where they have not diffused out of the substrate. In a specific embodiment, the concentration of hydrogen particles ranges

from about 10^{21} to about 5 X 10^{22} atoms/cm^3. Alternatively, the concentration of hydrogen particles is at least about 6 X 10^{21} atoms/cm^3. Depending upon the embodiment, the particular concentration of the hydrogen particles can be adjusted.

Still further in other embodiments, the present substrate undergoes a process of hydrogen treatment or implantation before thermal treatment purposes. Here, the substrate, including the detached film, is subjected to hydrogen bearing particles by way of implantation, diffusion, or any combination thereof. In some embodiments, where hydrogen has diffused out from the initial implant, a subsequent hydrogen treatment process can occur to increase a concentration of hydrogen in the detached film. The present hydrogen treatment process can occur for substrates made by way of other processes such as those noted below.

Moreover, the present technique for finishing the cleaved surface can use a combination of etchant, deposition, and thermal treatment to smooth the cleaved film. Here, the cleaved film is subjected to hydrogen bearing compounds such as HCl, HBr, HI, HF, and others. Additionally, the cleaved film is subjected to for example, deposition, during a time that the film is subjected to the hydrogen bearing compounds, which etch portions of the cleaved film. Using a silicon cleaved film for example, the deposition may occur by way of a silicon bearing compound such as silanes, e.g., $Si_xCl_yH_z$, SiH_4, $SiCl_x$, and other silicon compounds. Accordingly, the present method subjects the cleaved film to a combination of etching and deposition using a hydrogen bearing compound and a silicon bearing compound. Additionally, the cleaved surface undergoes thermal treatment while being subjected to the combination of etchant and deposition gases The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be from an epitaxial chamber, which has lamps for rapidly heating a substrate. In an embodiment using a silicon wafer and hydrogen gas, the tool can heat the substrate at a rate of about 10 Degrees Celsius/second and greater or 20 Degrees Celsius/second and greater, depending upon the embodiment.

An alternative embodiment will be described with reference to Figs. 21A to 21G. Numerals in Figs. 21A to 21G which are the same as those in Figs. 20A to 20E represent the same portions in Figs. 20A to 20E. In the embodiment shown in

Figs. 20A to 20E, the surfaces of the two substrates to be bonded are the SiO_2 layer 2903 and the SiO_2 layer 2904. However, both of these surfaces are not necessarily the SiO_2 layers, but at least one of them may be made of SiO_2. In this preferred embodiment, the surface of an epitaxial silicon layer 3102 formed on a porous silicon layer is bonded to the surface of an oxidized film 3104 formed on a silicon substrate 3110, and the surface of an oxidized film 3103 formed by thermal oxidation of the surface of the epitaxial silicon layer 3102 is bonded to the surface of the silicon substrate 3110 which is not oxidized. In this preferred embodiment, the other processes can be performed as in the embodiment shown in Figs. 20A to 20E.

An alternative embodiment will be described with reference to Figs. 22A to 22G. Numerals in Figs. 22A to 22G which are the same as those in Figs. 20A to 20E represent the same portions in Figs. 20A to 20E. In this preferred embodiment, a substrate bonded to a substrate formed with an epitaxial silicon film is made of a glass material 3210, such as quartz glass or blue glass. In this preferred embodiment, an epitaxial silicon layer 3102 is bonded to the glass substrate 3210, and an oxidized film 3103 formed by thermal oxidation of the surface of the epitaxial silicon layer 3102 is bonded to the glass substrate 3210. In this preferred embodiment, the other processes can be performed as in the embodiment shown in Figs. 20A to 20E.

Depending upon the embodiment, the present combination of thermal treatment and etching can be used to remove surface roughness of any of the detached films. The present invention can also use a combination of deposition, etching, and thermal treatment for other films in a porous film process. Further details of producing porous silicon materials are described in U.S. Patent No. 5,854,123, assigned to Canon Kabushiki Kaisha.

In a specific embodiment, the silicon-on-insulator substrate undergoes a series of process steps for formation of integrated circuits thereon. These processing steps are described in S. Wolf, Silicon Processing for the VLSI Era (Volume 2), Lattice Press (1990), which is hereby incorporated by reference for all purposes.

Although the above description is in terms of a silicon wafer, other substrates may also be used. For example, the substrate can be almost any monocrystalline, polycrystalline, or even amorphous type substrate. Additionally, the

substrate can be made of III/V materials such as gallium arsenide, gallium nitride (GaN), and others. The multi-layered substrate can also be used according to the present invention. The multi-layered substrate includes a silicon-on-insulator substrate, a variety of sandwiched layers on a semiconductor substrate, and numerous other types of substrates. Additionally, the embodiments above were generally in terms of providing a pulse of energy to initiate a controlled cleaving action. The pulse can be replaced by energy that is scanned across a selected region of the substrate to initiate the controlled cleaving action. Energy can also be scanned across selected regions of the substrate to sustain or maintain the controlled cleaving action. One of ordinary skill in the art would easily recognize a variety of alternatives, modifications, and variations, which can be used according to the present invention.

SMOOTHING METHOD USING THERMAL TREATMENT

According to yet another embodiment of the present invention, a thin film in a monocrystalline silicon wafer is produced with the aid of H+ ion implantations. The implantation of H+ ions (e.g., protons) at 150 keV in a monocrystalline silicon wafer, whose surface corresponds to a principle crystallographic plane, e.g., a 100 plane, leads in the case of weak implantation doses ($< 10^{16}$ atoms/cm ^{2}) to a hydrogen concentration profile C as a function of the depth P having a concentration maximum for a depth Rp, as shown in a diagram of Fig. 24. In the case of a proton implantation in silicon, Rp is approximately 1.25 micrometers. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many variations, alternatives, and modifications.

For doses of approximately 10^{16} atoms/cm ^{2}, the implanted hydrogen atoms start to form bubbles, which are distributed in the vicinity of a plane parallel to the surface. The plane of the surface corresponds to a principal crystallographic plane and the same applies with respect to the plane of the microbubbles, which is consequently a cleaving plane.

For an implanted dose of $> 10^{16}$ atoms/cm ^{2}, (e.g. 5×10^{16} atoms/cm ^{2}), it is possible to thermally trigger the coalescence between the bubbles inducing a

cleaving into two parts of the silicon, an upper 1.2 micrometer thick film (the thin film) and the mass of the substrate. Hydrogen implantation is an advantageous example, because the braking process of said ion in silicon is essentially ionization (electronic braking), the braking of the nuclear type with atomic displacements only occurring at the end of the range. This is why few defects are created in the surface layer of the silicon and the bubbles are concentrated in the vicinity of the depth Rp (depth of the concentration maximum) over a limited thickness. This makes it possible to obtain the necessary efficiency of the method for moderate implanted doses (5×10^{16} atoms/cm ^{2}) and, following the separation of the surface layer, a surface having a limited roughness, but such roughness should be taken out before the manufacture of integrated circuits. The use of the process according to the invention makes it possible to choose the thickness of the thin film within a wide thickness range by choosing the implantation energy. This property is more important as the implanted ion has a low atomic number z.

Fig. 25 shows the semiconductor wafer 3701 optionally covered with an encapsulating layer 3710 subject to an ion bombardment 3702 of H+ ions through the planar face 3704, which is parallel to a principal crystallographic plane. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. It is possible to see the microbubble layer 3703 parallel to the face 3704. The layer 3703 and the face 3704 define the thin film 3705. The remainder of the semiconductor substrate 3706 constitutes the mass of the substrate.

Fig. 26 shows a simplified diagram of the stiffener 3707 which is brought into intimate contact with the face 3704 of the semiconductor wafer 3701. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. In an interesting embodiment of the invention, ion implantation in the material takes place through a thermal silicon oxide encapsulating layer 3710 and the stiffener 3707 is constituted by a silicon wafer covered by at least one dielectric layer. Another embodiment uses an electrostatic pressure for fixing the stiffener to the semiconductor material. In this case, a silicon stiffener is chosen having an e.g. 5000 Angstrom thick

silicon oxide layer. The planar face of the wafer is brought into contact with the oxide of the stiffener and between the wafer and the stiffener is applied a potential difference of several dozen volts. The pressures obtained are then a few 10^5 to 10^6 Pascal.

Fig. 27 shows a simplified diagram of the film 3705 joined to the stiffener 3707 separated by the space 3708 from the mass of the substrate 3706. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The diagram shows that the film is separated from the mass of the substrate. The surface of the film is generally rough and often requires additional processing.

Fig. 28 is a simplified diagram of a removed film attached to a stiffener according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The film has an upper cleaved surface 3709, which generally has a certain roughness. The roughness is often greater than that which is generally acceptable for manufacturing integrated circuits. In silicon wafers, for example, the surface roughness can be greater than about 10 nanometers root mean square ("RMS") or greater. Alternatively, the surface roughness is about 2-8 nanometers root mean square and greater. During the cleaving process, most of the hydrogen has escaped. However, it is possible that a portion of the hydrogen, even a substantial portion of the hydrogen remain in the detached film. In some embodiments, the roughness can be polished by way of mechanical processes such as chemical mechanical planarization, touch polishing, and the like. Alternatively, the mechanical polishing process can be used alone or even combined with chemical processes, which will be described more fully below.

Fig. 29 is a simplified diagram of a smoothed film attached to a stiffener according to an embodiment of the present invention. This diagram is merely an example, which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, alternatives, and modifications. To smooth or treat surface 3709, the substrate is subjected to thermal and chemical treatment 3713. In particular, the substrate is also subjected to an etchant including a

halogen bearing compound such as HCl, HBr, HI, HF, and others. The etchant can also be a fluorine bearing compound such as SF_6, C_xF_x.

In preferred embodiments, the present substrate undergoes treatment using a combination of etchant and thermal treatment in a hydrogen bearing environment. In a specific embodiment, the etchant is HCl gas or the like. The thermal treatment uses a hydrogen etchant gas. In some embodiments, the etchant gas is a halogenated gas, e.g., HCl, HF, HI, HBr, SF_6, CF_4, NF_3, and CCl_2F_2. The etchant gas can also be mixed with another halogen gas, e.g., chlorine, fluorine. The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be from an epitaxial chamber, which has lamps for rapidly heating a substrate. In an embodiment using a silicon wafer and hydrogen gas, the tool can heat the substrate at a rate of about 10 Degrees Celsius/second and greater or 20 Degrees Celsius/second and greater, depending upon the embodiment.

In one embodiment, it is believed that the hydrogen particles in the detached surface improves the surface smoothing process. Here, the hydrogen particles have been maintained at a temperature where they have not diffused out of the substrate. In a specific embodiment, the concentration of hydrogen particles ranges from about 10^{21} to about 5×10^{22} atoms/cm^3. Alternatively, the concentration of hydrogen particles is at least about 6×10^{21} atoms/cm^3. Depending upon the embodiment, the particular concentration of the hydrogen particles can be adjusted.

Still further in other embodiments, the present substrate undergoes a process of hydrogen treatment or implantation before thermal treatment purposes. Here, the substrate, including the detached film, is subjected to hydrogen bearing particles by way of implantation, diffusion, or any combination thereof. In some embodiments, where hydrogen has diffused out from the initial implant, a subsequent hydrogen treatment process can occur to increase a concentration of hydrogen in the detached film. A finished wafer after smoothing or surface treatment is shown in the Fig. Here, the finished wafer includes a substantially smooth surface 3711, which is generally good enough for the manufacture of integrated circuits without substantial polishing or the like.

Moreover, the present technique for finishing the cleaved surface can use a combination of etchant, deposition, and thermal treatment to smooth the cleaved film. Here, the cleaved film is subjected to hydrogen bearing compounds such as HCl, HBr, HI, HF, and others. Additionally, the cleaved film is subjected to for example, deposition, during a time that the film is subjected to the hydrogen bearing compounds, which etch portions of the cleaved film. Using a silicon cleaved film for example, the deposition may occur by way of a silicon bearing compound such as silanes, e.g., $Si_xCl_yH_z$, SiH_4, $SiCl_x$, and other silicon compounds. Accordingly, the present method subjects the cleaved film to a combination of etching and deposition using a hydrogen bearing compound and a silicon bearing compound. Additionally, the cleaved surface undergoes thermal treatment while being subjected to the combination of etchant and deposition gases The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be from an epitaxial chamber, which has lamps for rapidly heating a substrate. In an embodiment using a silicon wafer and hydrogen gas, the tool can heat the substrate at a rate of about 10 Degrees Celsius and greater or 20 Degrees Celsius and greater, depending upon the embodiment. The temperature can be maintained at about 1000 to about 1200 Degrees Celsius and greater. The substrate can also be maintained at a pressure of about 1 atmosphere, but is not limiting.

In a further embodiment, the present method can also include an epitaxial deposition step following the smoothing step. The deposition step can form epitaxial silicon or other materials overlying the film. In a specific embodiment, the silicon-on-insulator substrate undergoes a series of process steps for formation of integrated circuits thereon. These processing steps are described in S. Wolf, Silicon Processing for the VLSI Era (Volume 2), Lattice Press (1990), which is hereby incorporated by reference for all purposes.

Although the above has been generally described in terms of a PIII system, the present invention can also be applied to a variety of other plasma systems. For example, the present invention can be applied to a plasma source ion implantation system. Alternatively, the present invention can be applied to almost any plasma system where ion bombardment of an exposed region of a pedestal occurs.

Accordingly, the above description is merely an example and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, alternatives, and modifications.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method of fabricating a substrate, said method comprising providing a donor substrate comprising an upper surface;

introducing a plurality of particles through said upper surface and into said donor substrate to a selected depth beneath said upper surface to define a thickness of material of said donor substrate from said upper surface to said selected depth, said plurality of particles being defined by a distribution along said selected depth;

introducing energy to said donor substrate to initiate a cleaving action to free said thickness of material from said donor substrate to define a cleaved surface from said donor substrate, said cleaved surface comprising a surface roughness of a predetermined value and comprising a portion of said distribution of said plurality of particles; and

applying a combination of thermal treatment and an etchant to said cleaved surface and said portion of said distribution of said plurality of particles to reduce said surface roughness of said predetermined value.

2. The method of claim 1 wherein said thermal treatment increases a temperature of said cleaved surface to about 1,000 Degrees Celsius and greater.

3. The method of claim 1 wherein said plurality of particles comprise a hydrogen bearing species.

4. The method of claim 1 wherein said reduced predetermined value is less than about 1 nanometers root mean square.

5. The method of claim 1 wherein said etchant comprising a halogen bearing compound is selected from at least Cl_2, HCl, HBr, HI, and HF.

6. The method of claim 1 wherein said etchant comprises a fluorine bearing compound.

7. A method of fabricating a substrate, said method comprising providing a silicon substrate comprising an upper surface;

introducing a plurality of particles through said upper surface and into said donor substrate to a selected depth beneath said upper surface to define a thickness of material of said donor substrate from said upper surface to said selected depth, said plurality of particles being defined by a distribution along said selected depth;

introducing energy to said donor substrate to initiate a cleaving action to free said thickness of material from said donor substrate to define a cleaved surface from said donor substrate, said cleaved surface comprising a surface roughness of a predetermined value and comprising a portion of said distribution of said plurality of particles; and

applying a combination of thermal treatment using rapid thermal processing and an etchant comprising a hydrogen bearing compound to said cleaved surface and said portion of said distribution of said plurality of particles to reduce said surface roughness of said predetermined value.

8. The method of claim 7 wherein said applying further comprising applying a film to said cleaved surface.

9. A semiconductor substrate producing method comprising:

forming a first porous silicon layer on at least one surface of a silicon substrate; and

forming a second layer having a larger porosity than the first porous silicon layer at a constant depth from a surface of said porous silicon in said first porous silicon layer, said second layer forming step comprising implanting ions into said first porous silicon layer with a given projection range;

bonding said non-porous layer and a support substrate together;

separating said silicon substrate into two portions at said second layer to remove the porous silicon layer exposed on a surface of said support substrate and exposing said non-porous layer; and

smoothing the non-porous layer by subjecting surfaces of the non-porous layer using an etchant species and thermal treatment.

10. The semiconductor substrate producing method according to claim 9 further comprising a non-porous layer forming step for forming a non-porous layer on a surface of said first porous layer before said ion implanting step.

11. The semiconductor substrate producing method according to claim 29 wherein said non-porous layer is made of single-crystal silicon having an oxidized silicon layer on a surface to be bonded.

12. A semiconductor substrate producing method comprising: .

forming on a surface of a silicon substrate a first porous silicon layer;

implanting ions into the first porous silicon layer to form a second porous silicon layer having a porosity higher than the first porous silicon layer at a constant depth from a surface of the first porous silicon layer;

forming a non-porous monocrystalline semiconductor layer on the first porous silicon layer;

bonding the non-porous monocrystalline semiconductor layer located on the silicon substrate to another substrate;

separating the silicon substrate and the other substrate at the second porous silicon layer so that the non-porous monocrystalline semiconductor layer remains on the other substrate; and

applying a combination of thermal treatment and an etchant to a surface of the non-porous monocrystalline semiconductor layer to reduce a surface roughness to a predetermined value.

13. The method of claim 12 wherein the thermal treatment increases a temperature of the to about 1,000 Degrees Celsius and greater.

14. The method of claim 12 wherein the temperature increases is about 10 Degrees Celsius per second and greater.

15. A method for the preparation of thin semiconductor material films, wherein the process comprises subjecting a semiconductor material wafer having a planar face and whose plane, is substantially parallel to a principal crystallographic plane, the method comprising:

implanting by ion bombardment of the face of said wafer by means of ions creating in the volume of said wafer at a depth close to the average penetration depth of said ions, a layer of gaseous microbubbles defining in the volume of said wafer a lower region constituting a majority of the substrate and an upper region constituting the thin film, the temperature of the wafer during implantation being kept below the temperature

at which the gas produced by the implanted ions can escape from the semiconductor by diffusion;

contacting the planar face of said wafer with a stiffener constituted by at least one rigid material layer;

treating the assembly of said wafer and said stiffener at a temperature above that at which the ion bombardment takes place and adequate to create by a crystalline rearrangement effect in the wafer and a pressure effect in the microbubbles, a separation between the thin film and the majority of the substrate, the stiffener and the planar face of the wafer being kept in intimate contact during said stage to free the thin film from the majority of the substrate; and

applying a combination of thermal treatment and an etchant to said thin film to reduce a surface roughness of said thin film to a predetermined value.

16. The method of claim 15 wherein said ions are derived from hydrogen gas.

17. The method of claim 15 wherein said predetermined value is less than about 1 nanometers root mean square.

18. The method of claim 15 wherein said predetermined value is less than about 0.1 nanometer root mean square.

19. The method of claim 15 wherein said etchant comprising a halogen bearing compound is selected from at least Cl_2, HCl, HBr, HI, and HF.

20. The method of claim 15 wherein said etchant comprises a fluorine bearing compound.

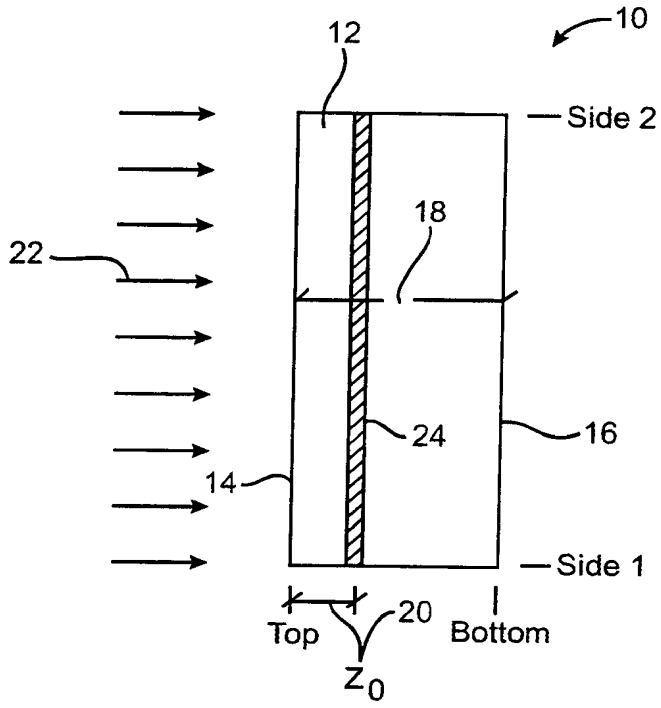

10
12
Side 2
18
22
24
16
14
Side 1
Top
20
Bottom
Z_0

FIG. 1

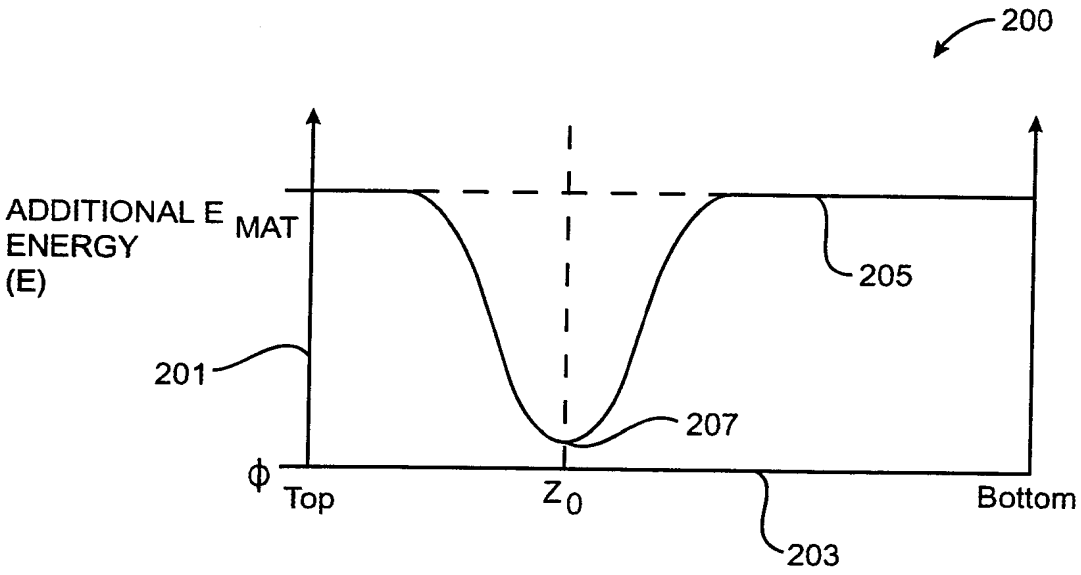

200
ADDITIONAL E
ENERGY
(E)
MAT
205
201
207
ϕ
Top
Z_0
Bottom
203

FIG. 2

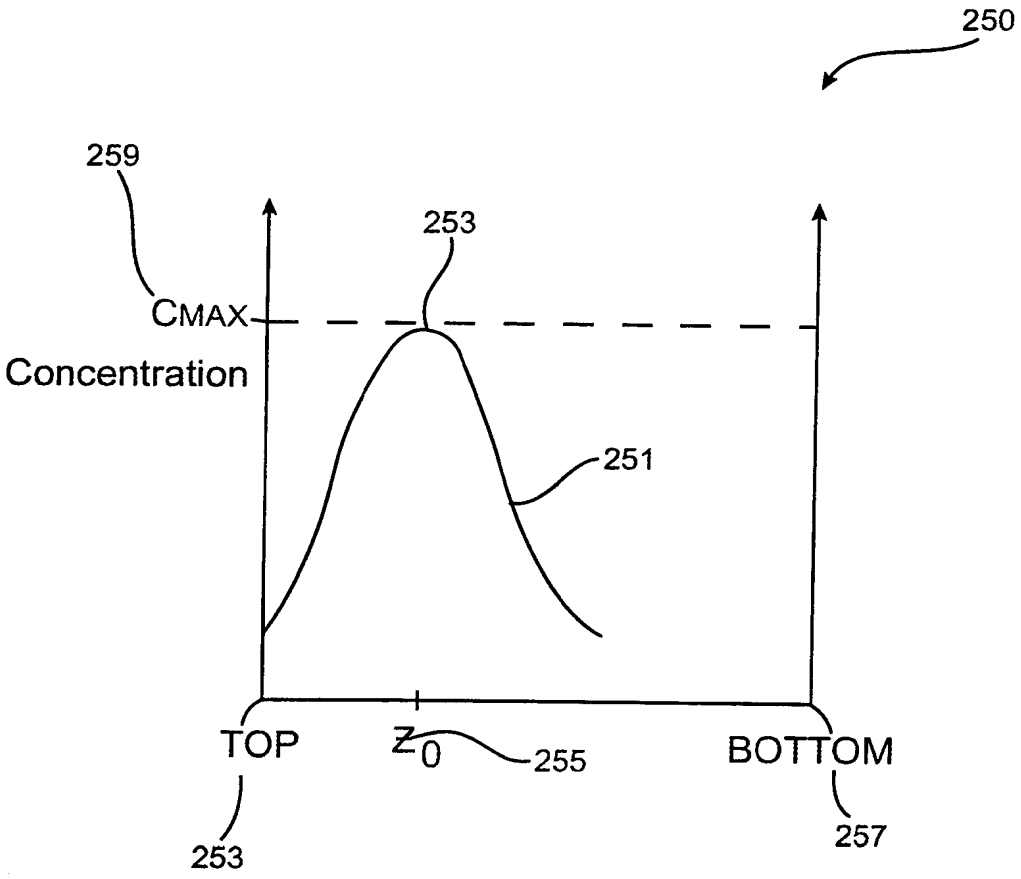


FIG. 1A

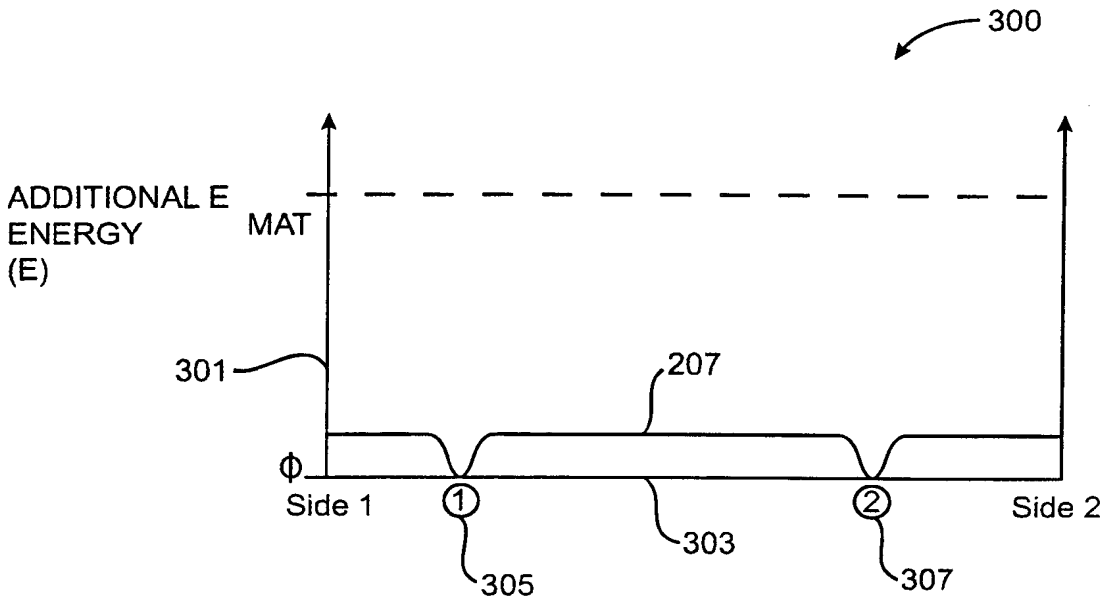

300
ADDITIONAL E
ENERGY
(E)
MAT
301
207
ϕ
Side 1
1
2
Side 2
303
305
307

FIG. 3

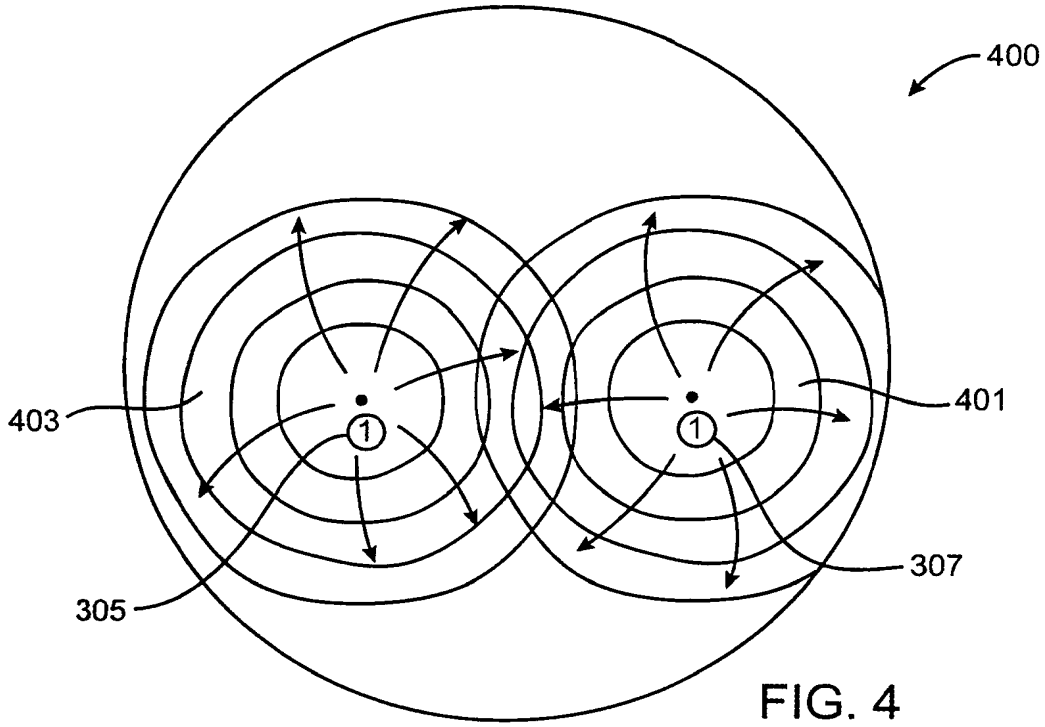

400
403
401
1
1
305
307

FIG. 4

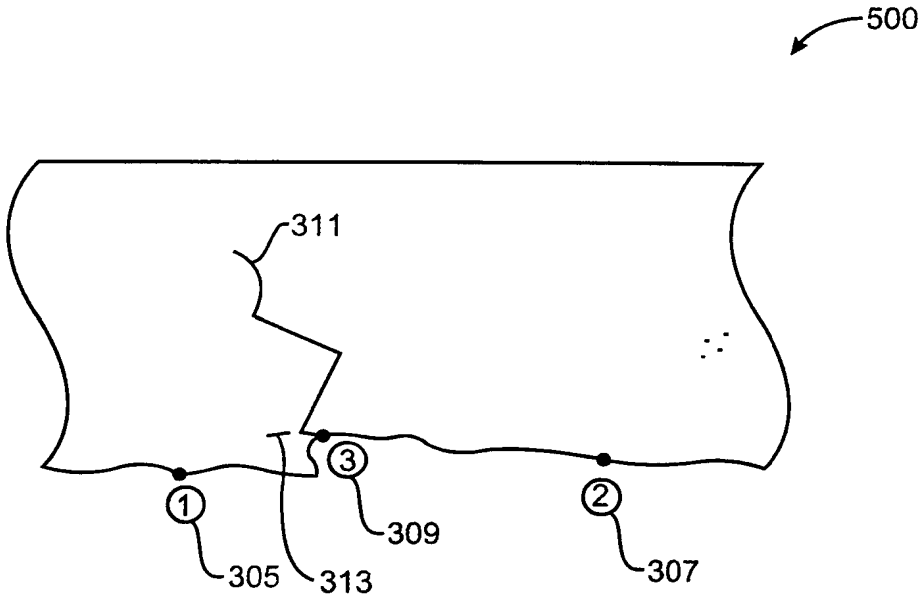


FIG. 5

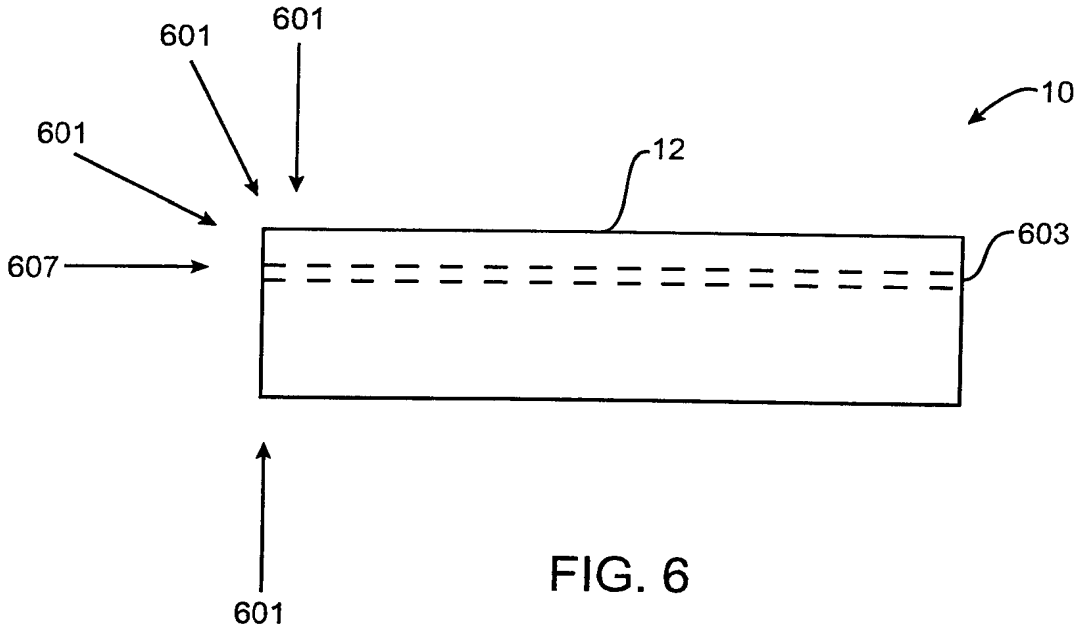

601
601
601
10
12
603
607
601

FIG. 6

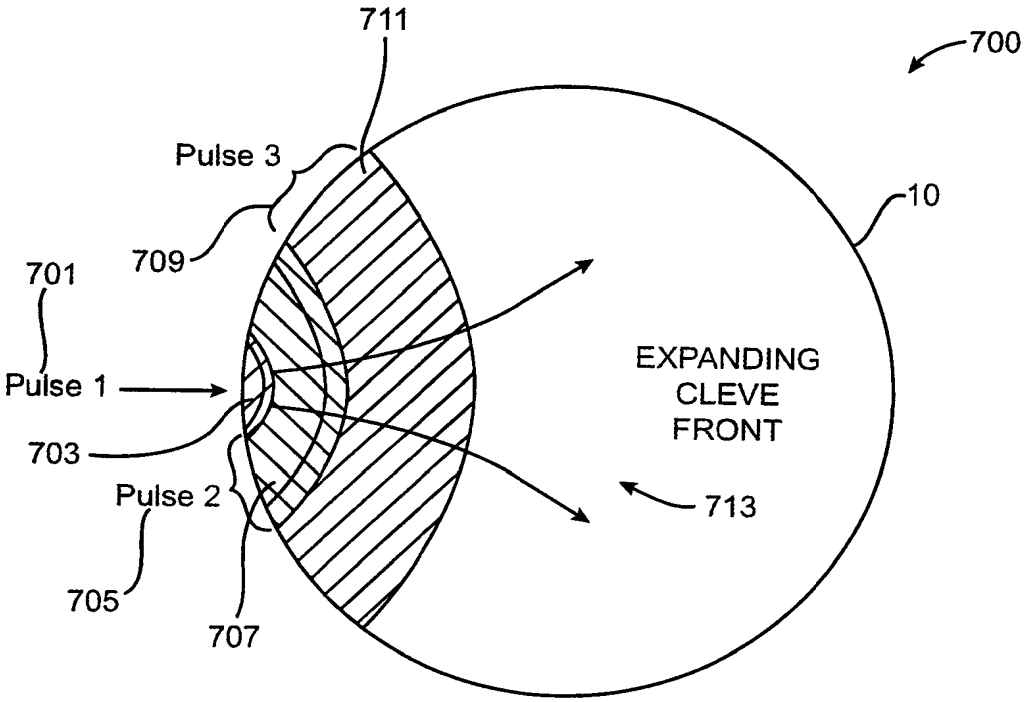

711
700
Pulse 3
10
709
701
EXPANDING
CLEVE
FRONT
Pulse 1
703
Pulse 2
713
705
707

FIG. 7

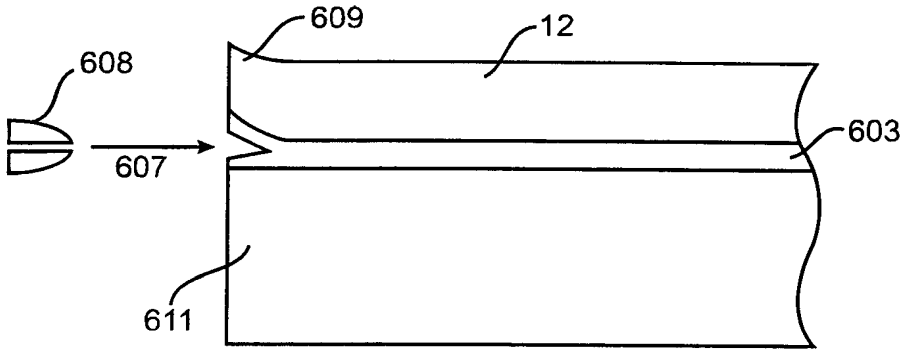

609
12
608
603
607
611

FIG. 6A

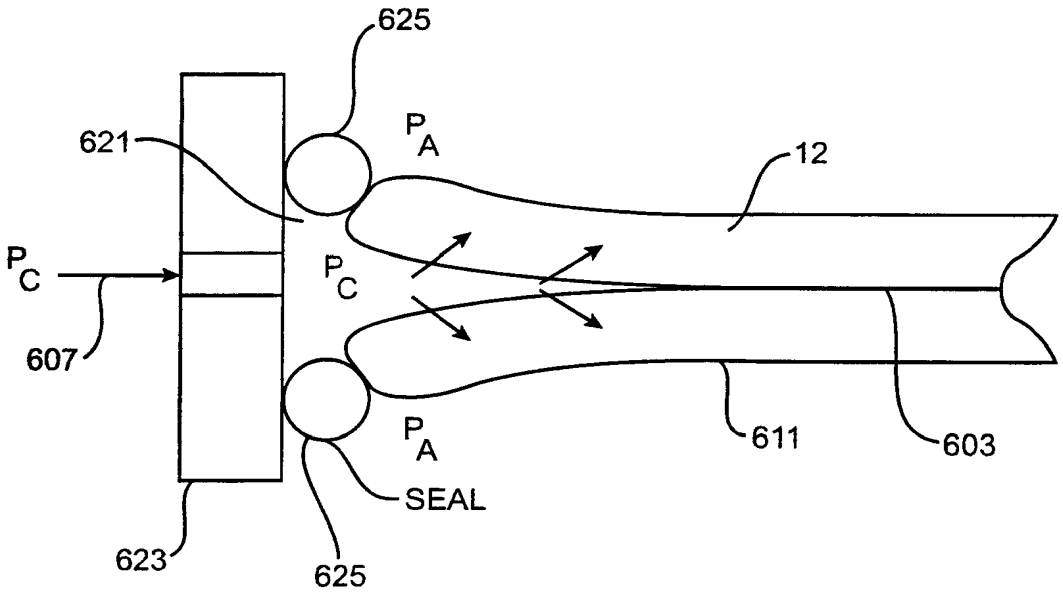

625
621
P_A
12
P_C
P_C
607
P_A
611
603
SEAL
623
625

FIG. 6B

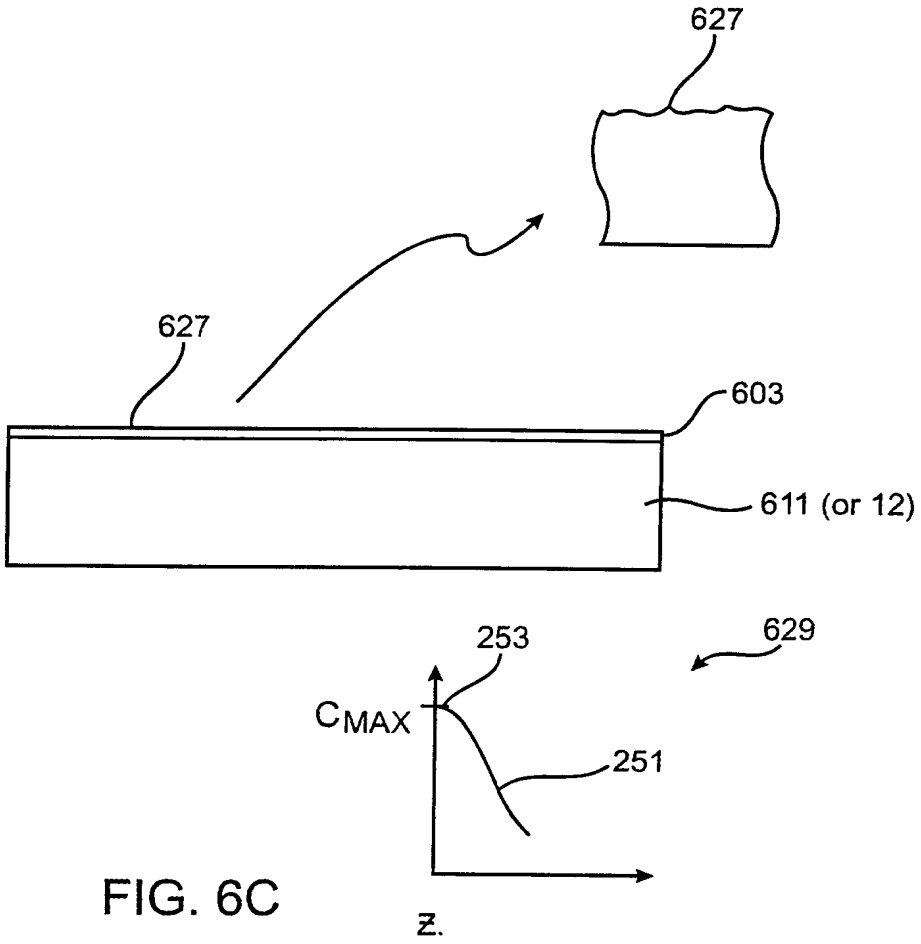


FIG. 6C

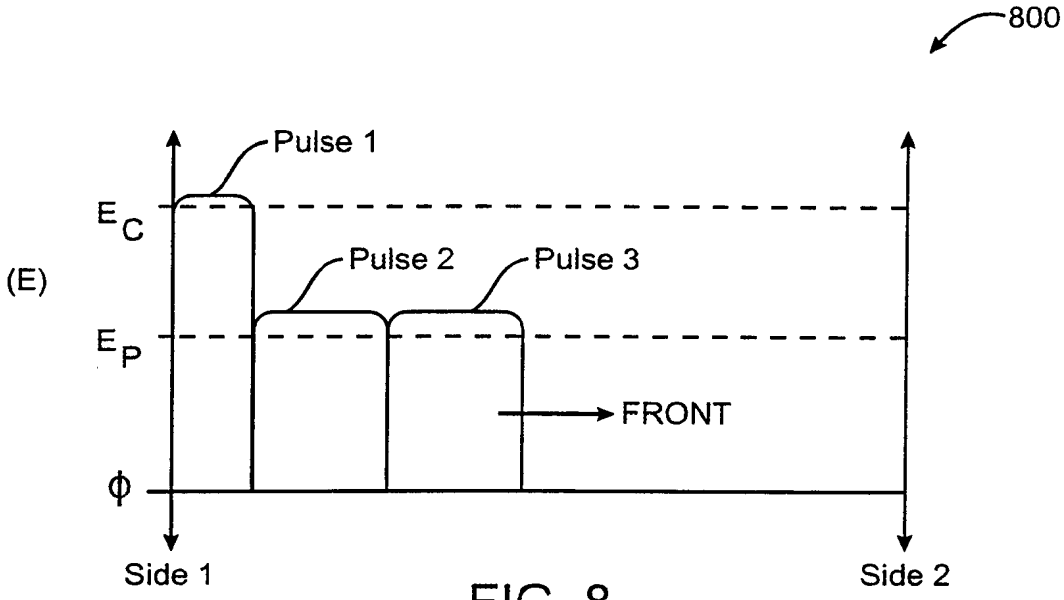

800
Pulse 1
E_C
(E)
Pulse 2
Pulse 3
E_P
FRONT
ϕ
Side 1
Side 2

FIG. 8

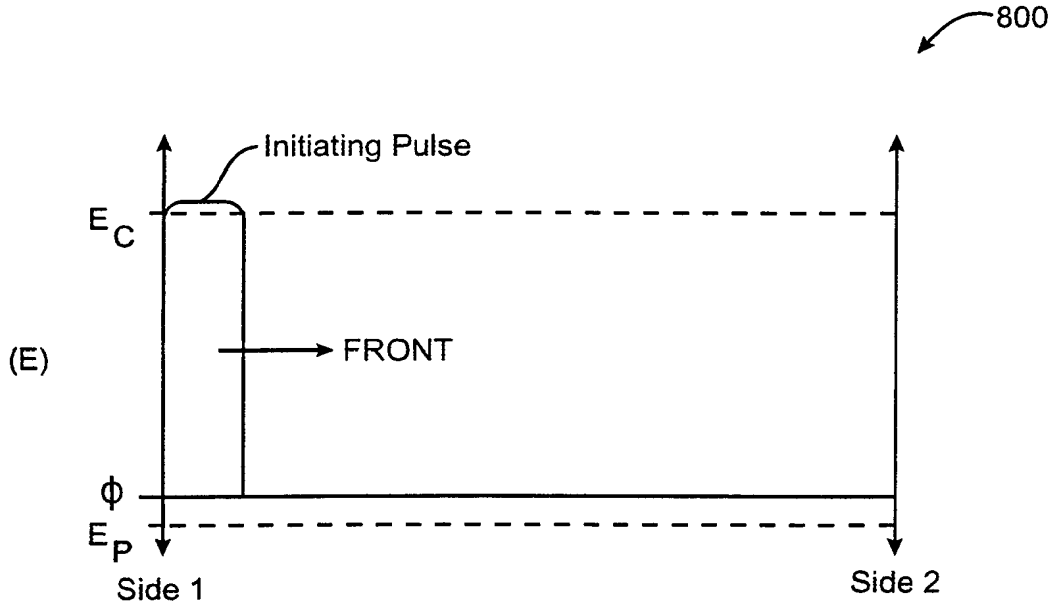

800
Initiating Pulse
E_C
(E)
FRONT
ϕ
E_P
Side 1
Side 2

FIG. 9

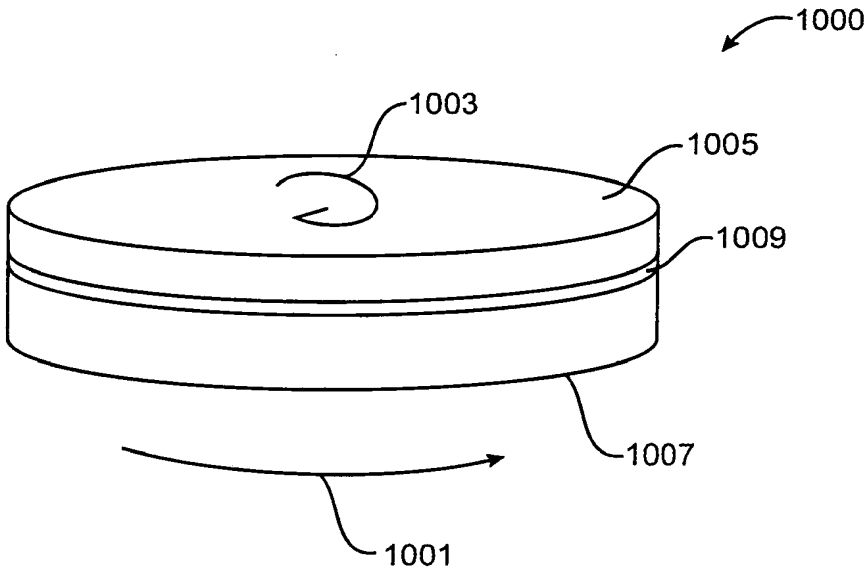

1000
1003
1005
1009
1007
1001

FIG. 10

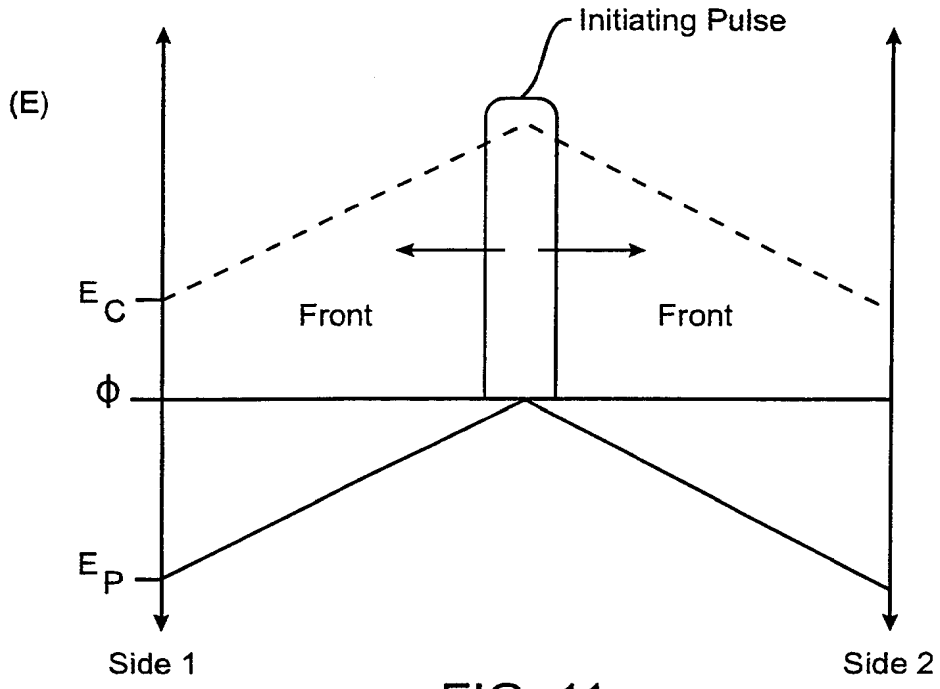

Initiating Pulse
(E)
E C
Front
Front
ϕ
E P
Side 1
Side 2

FIG. 11

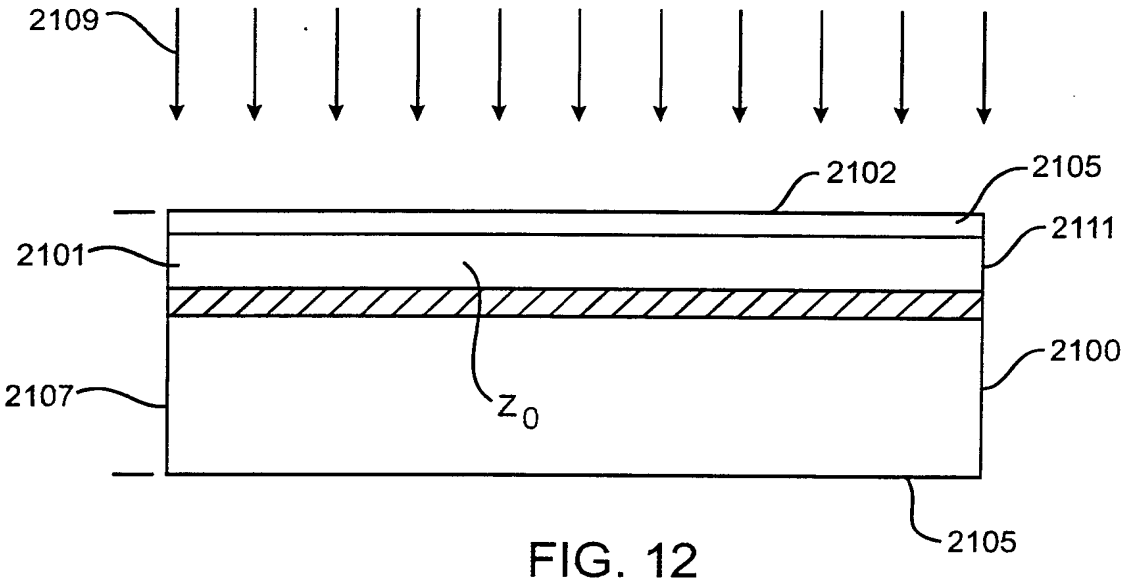

2109
2102
2105
2111
2101
2100
2107
Z_0
2105

FIG. 12

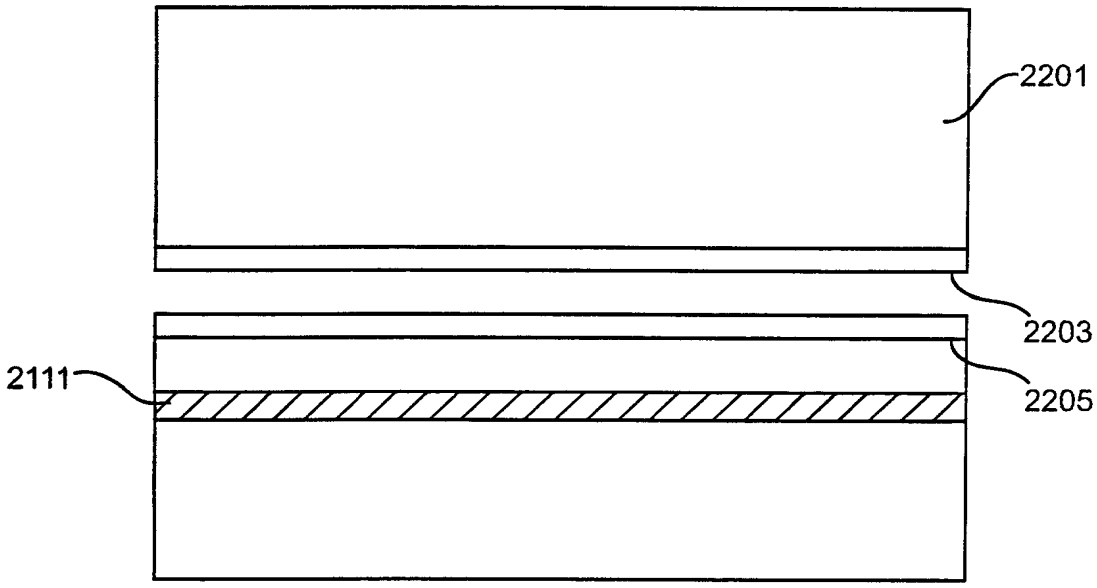

2201
2203
2111
2205

FIG. 13

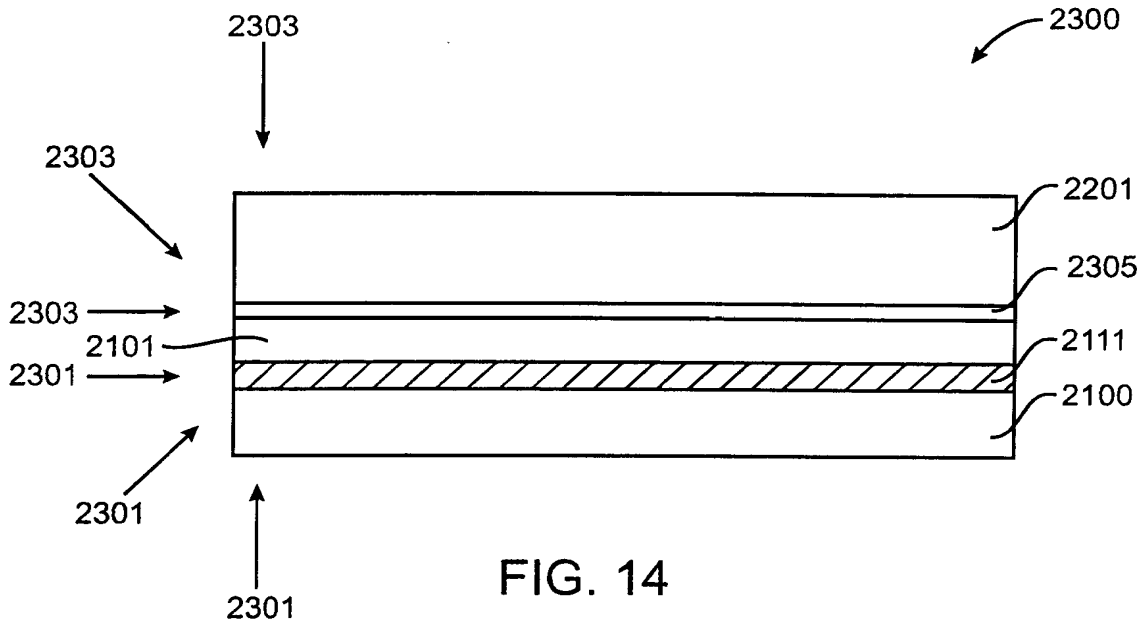

2303
2300
2303
2201
2305
2303
2101
2111
2301
2100
2301
2301

FIG. 14

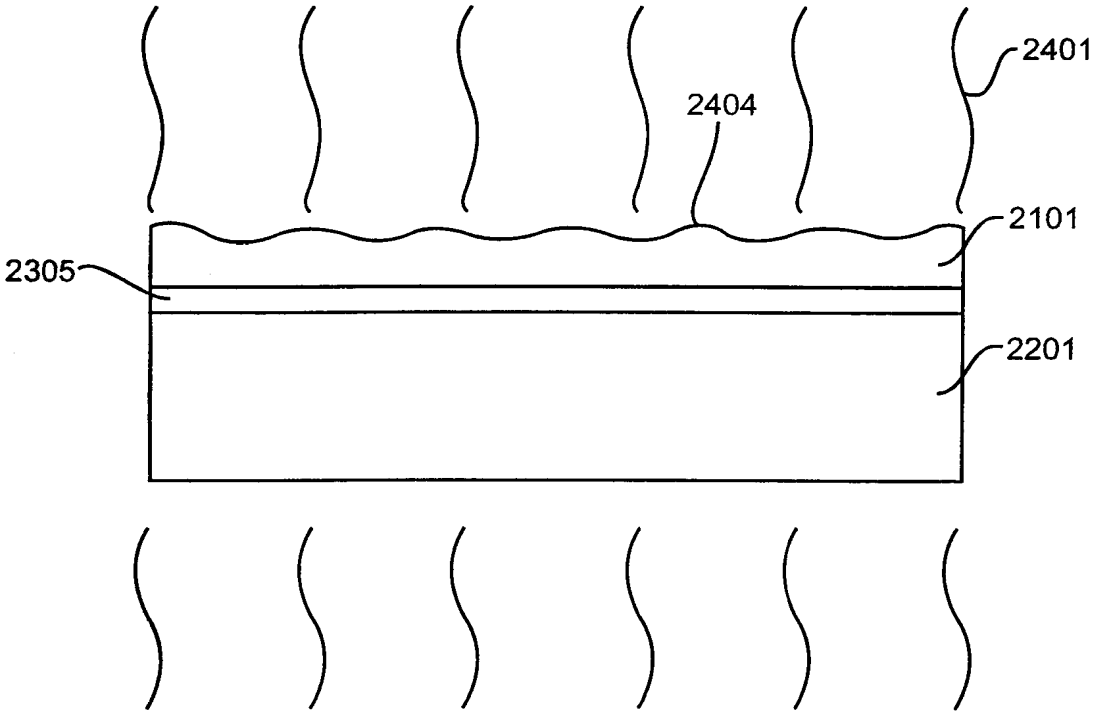

2401
2404
2101
2305
2201

FIG. 15

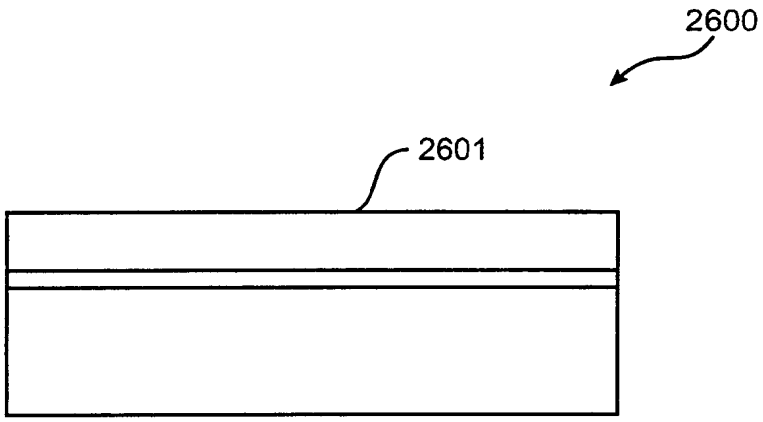


FIG. 16

FIG.17A

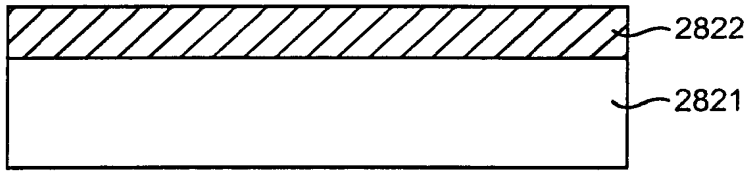


FIG.17B

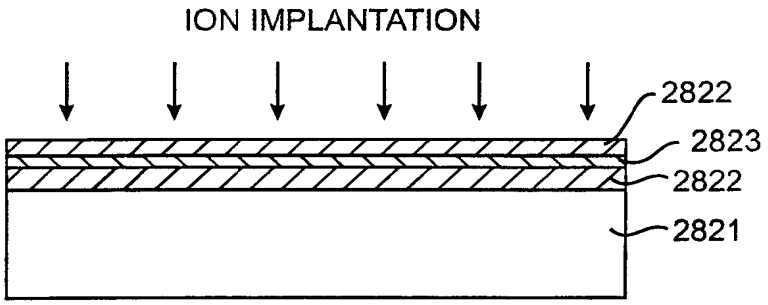


FIG.17C

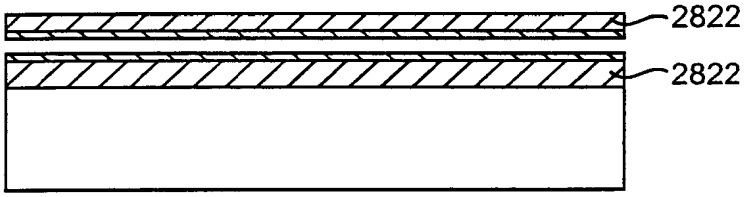


FIG.17D

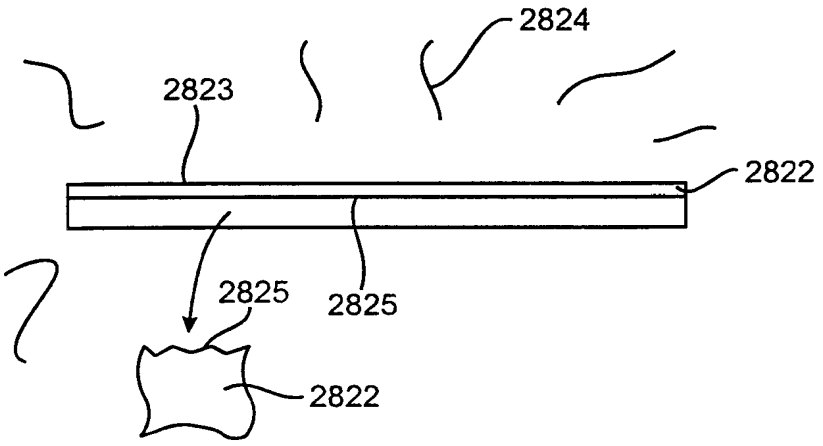


FIG. 18A

FIG. 18B

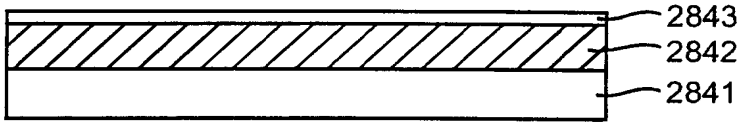


FIG. 18C

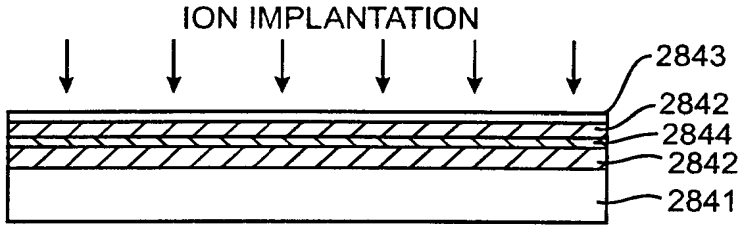


FIG. 18D

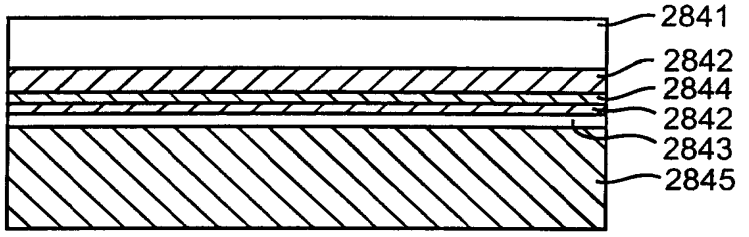


FIG. 18E

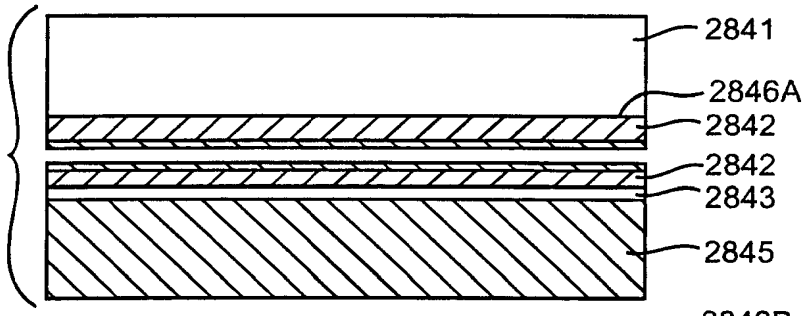


FIG. 18F

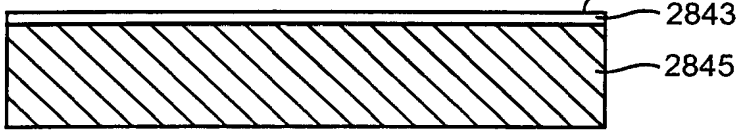


FIG. 18G

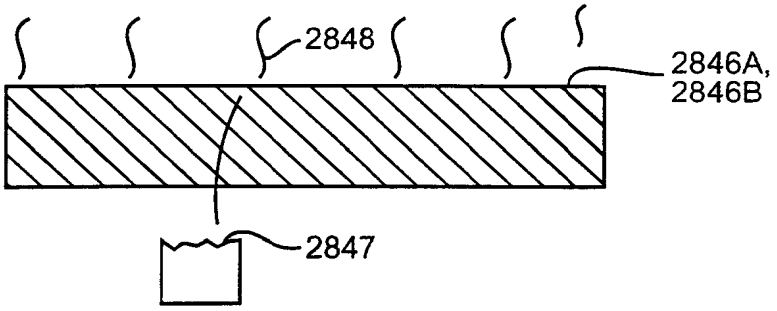


FIG. 19A

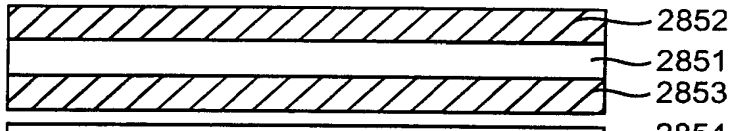


FIG. 19B

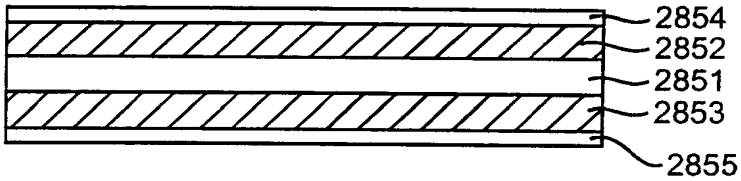


FIG. 19C

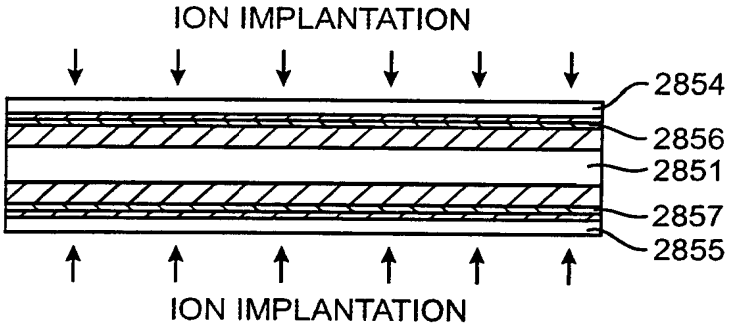


FIG. 19D

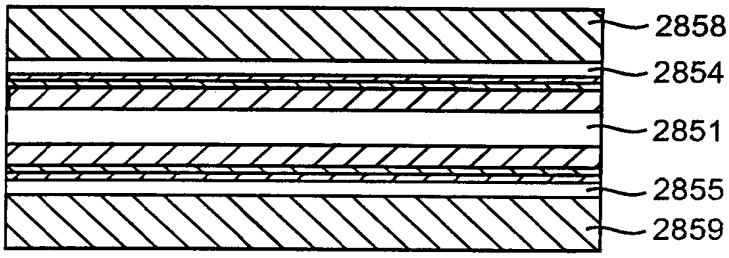


FIG. 19E

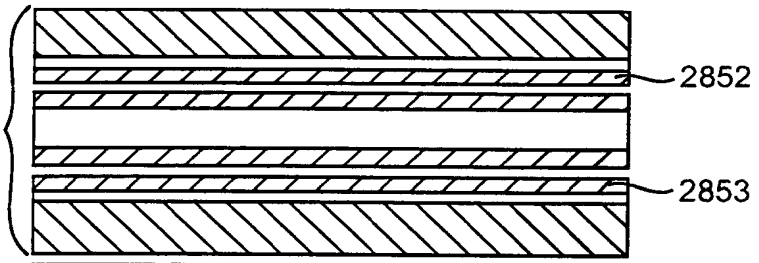


FIG. 19F

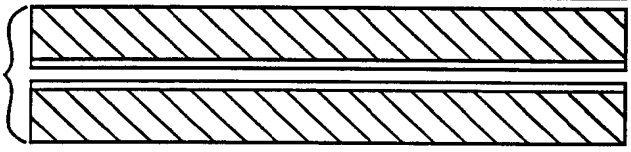


FIG. 20A

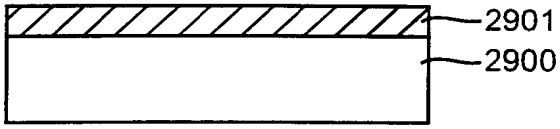


FIG. 20B

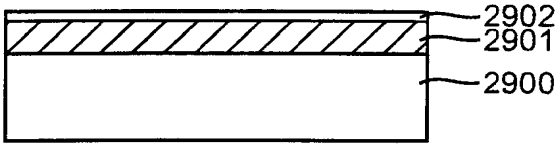


FIG. 20C

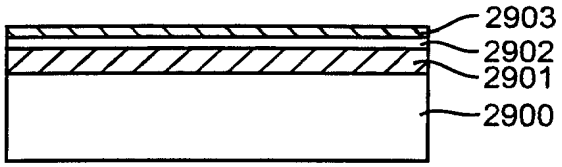


FIG. 20D

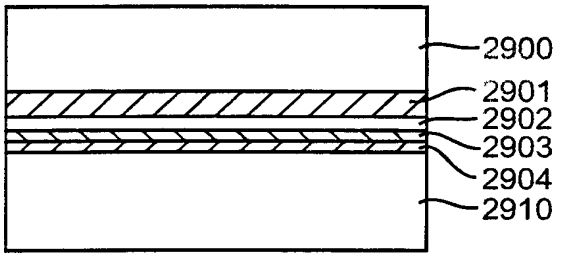


FIG. 20E

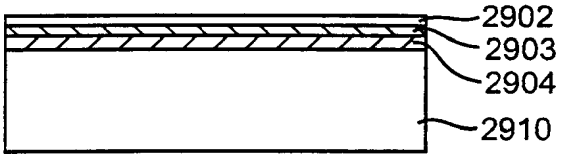


FIG. 21A

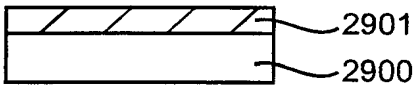


FIG. 21B

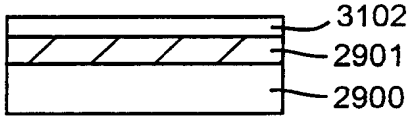


FIG. 21C

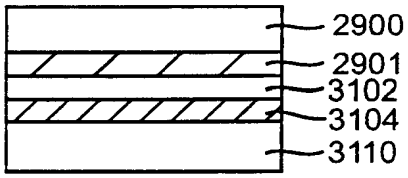


FIG. 21D

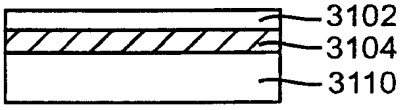


FIG. 21E

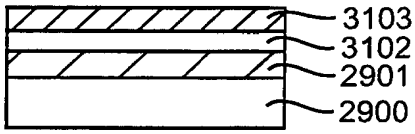


FIG. 21F

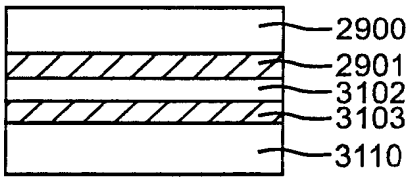


FIG. 21G

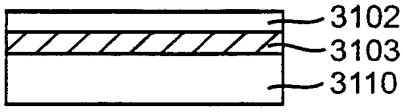


FIG. 22A

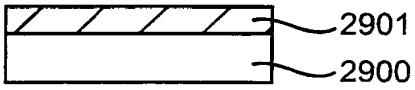


FIG. 22B

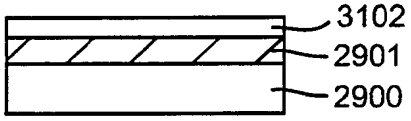


FIG. 22C

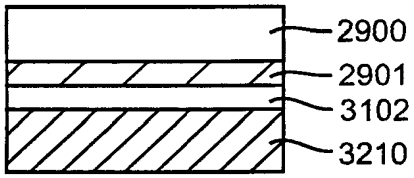


FIG. 22D

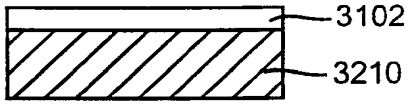


FIG. 22E

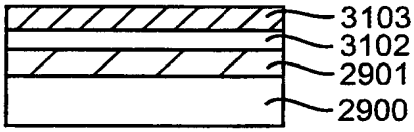


FIG. 22F

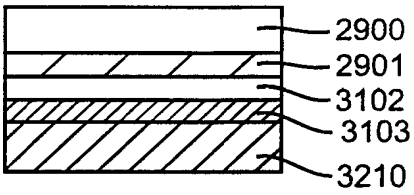


FIG. 22G

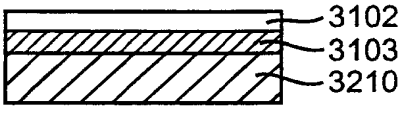


FIG. 23A

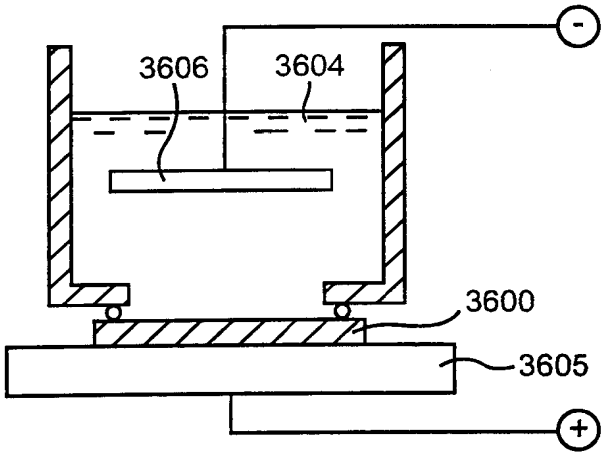
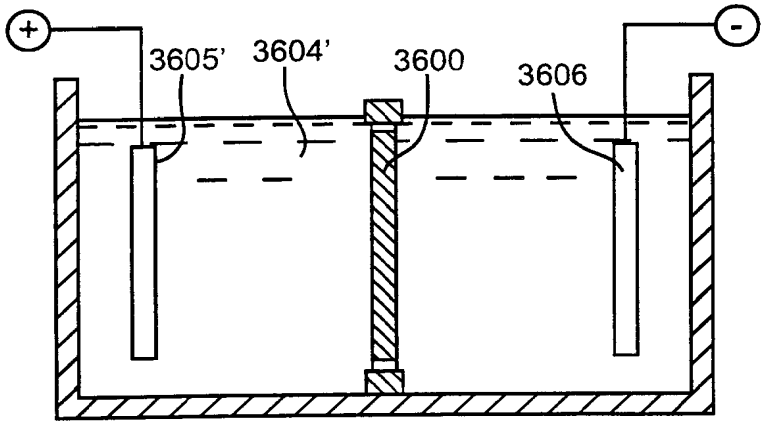


FIG. 23B



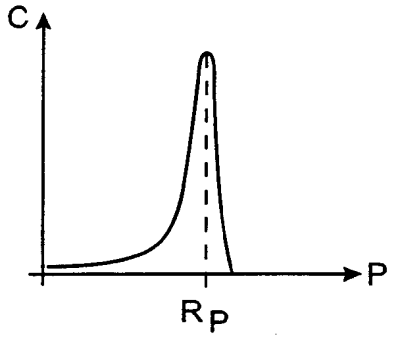


FIG. 24

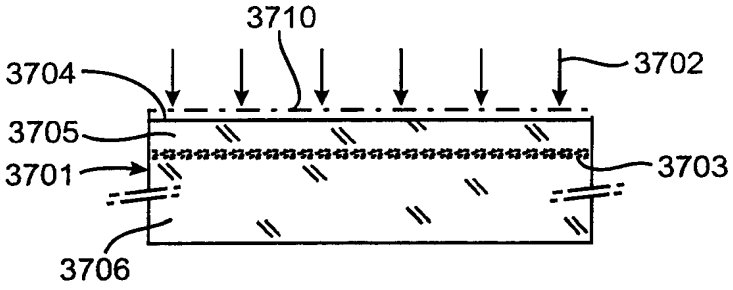


FIG. 25

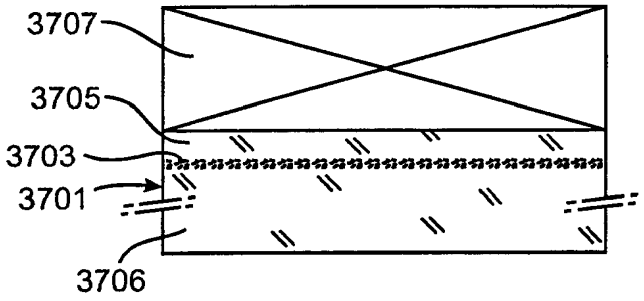


FIG. 26

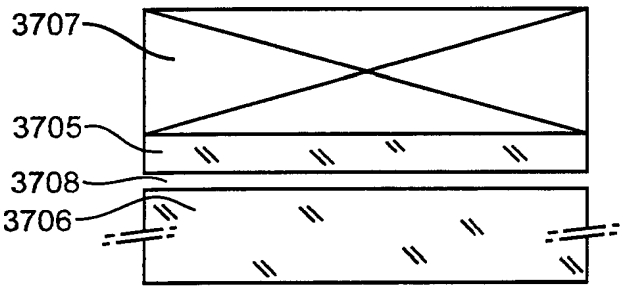


FIG. 27

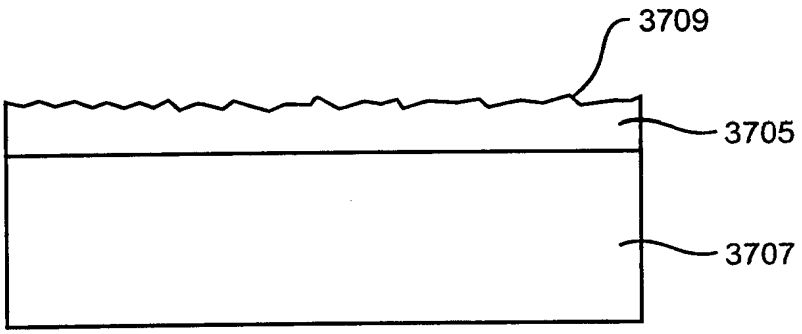


FIG. 28

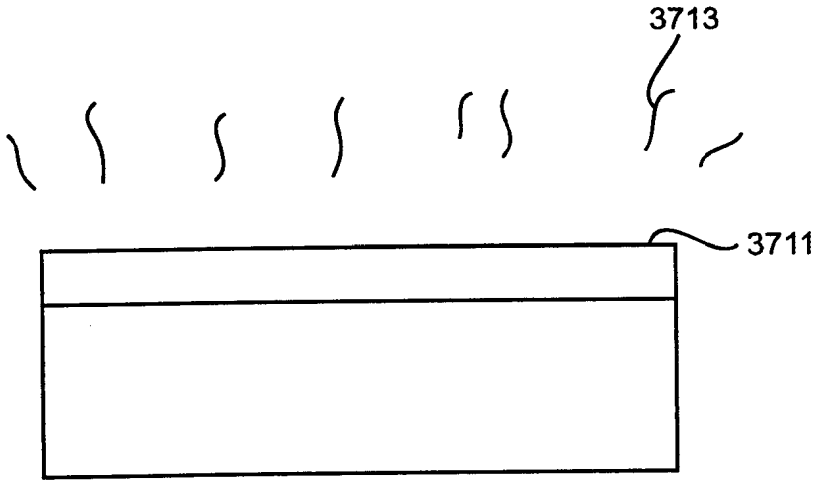


FIG. 29

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/10821

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 21/76, 21/30, 21/46, 21/78 21/301, 21/332, 21/31, 21/469
US CL : 438/460, 405, 455, 695, 780, 476

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/460, 405, 455, 695, 780, 476

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

BRS, MICROBUBBLES, THERMAL TREATMENT, HYDROGEN IONS, ETCHANT, FLUORIDE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,374,564 A (BRUEL) 20 December 1994, (20/12/94) col. 5 line 8-col. 6 line 12.	1-20
Y	US 4,495,219 A (KATO et al) 22 January 1985, (22/01/85) col. 4, lines 21-27, col. 6 lines 3-7.	1-20
Y	US 5,686,980 A (Hirayama et al) 11 November 1997, (11/11/97) col. 8 lines 41-51.	6, 20
A	US 3,964,957 A (Walsh) 22 June 1976, (22/06/76) col. 8 line 17-col. 9 line 10.	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 16 JUNE 2000	Date of mailing of the international search report 06 JUL 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer WALTER L. LINDSAY JR. Telephone No. (703) 308-0956